

MODEL NAME : QAR00

PCB NO : LA-7931P (DAA00002T00)

BOM P/N : 4319FN31L01
4319FN31L02

Compal Confidential

Vans 15

rPGA Ivy Bridge + FCBGA PCH Panther Point + MXM type A x1

Rev: 1.0 (A00)

2012.06.07

@ : Nopop component

CONN@ : ME connector

5@ : 6-bit LCD panel

6@ : 10-bit LCD panel

1@, 2@, 3@, 4@ : for TPM / TCM

PXDP@, JTAG@ : Total debug connector (pop them until ST)

MB Type	BOM P/N	Include 6-bit
TPM	4319FN31L01	1@ 3@ 5@ PXDP@ JTAG@

MB Type	BOM P/N	Include 10-bit
TPM	4319FN31L02	1@ 3@ 6@ PXDP@ JTAG@

SATA Re-driver (U26,U637)	Source	X76 P/N	Page
PS8520B (SA00004WF00)	main source	X7641231L01	35,43
MAX4951C (SA00002EY1L)	2nd source	X7641231L02	

USB3 Re-driver (U638)	Source	X76 P/N	Page
PS8720B (SA00004UI00)	main source	X7641231L03	40
PS8720A (SA00005PO00)	2nd source	X7641231L04	

ROM part	Source	X76 P/N	Page
U52 (SA000039A2L) U53 (SA00003K80L)	main (Winbond)	X7640631L01	17
U52 (SA000046400) U53 (SA00004LI00)	2nd (EON)	X7640631L03	

MB PCB

Part Number	Description
DAA00002T00	PCB OFE LA-7931P REV0 M/B DIS

power CKT: 05/17

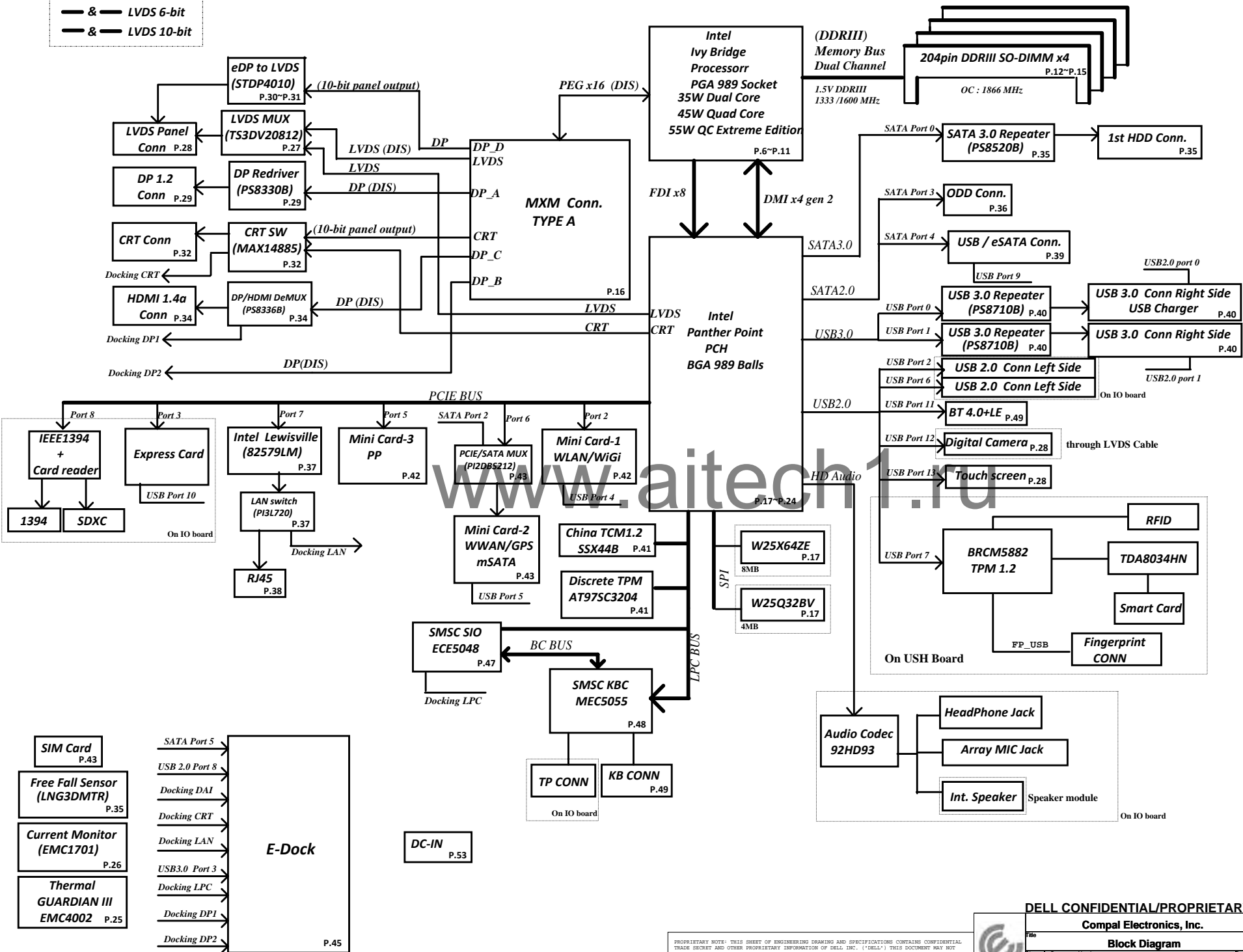
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Cover Sheet			
Title	LA-7931P		
Size	Document Number	Rev	1.0
Date	Monday, July 23, 2012	Sheet	1 of 70



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Block Diagram

LA-7931P

Rev	1.0
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Date: Monday, July 23, 2012 Sheet 2 of 70

POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M1	LOW	LOW	HIGH	LOW	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M1	LOW	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+15V_ALW +5V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

SATA	DESTINATION
SATA 0	HDD 1
SATA 1	NA
SATA 2	mSATA
SATA 3	ODD
SATA 4	ESATA
SATA 5	Dock

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Ext Right Side) USB3.0
	1	JUSB2 (Ext Right Side) USB3.0
	2	IO Board- JUSB1 (Ext Left Side)
	3	Docking USB3.0
	4	Docking USB 2.0
	5	WWAN
	6	IO Board- JUSB2 (Ext Left Side)
	7	USH
	8	WLAN
	9	ESATA
	10	Express Card
	11	BT 4.0
	12	Camera
	13	Touch Screen
USH	0	BIO
	1	NA

Stack up

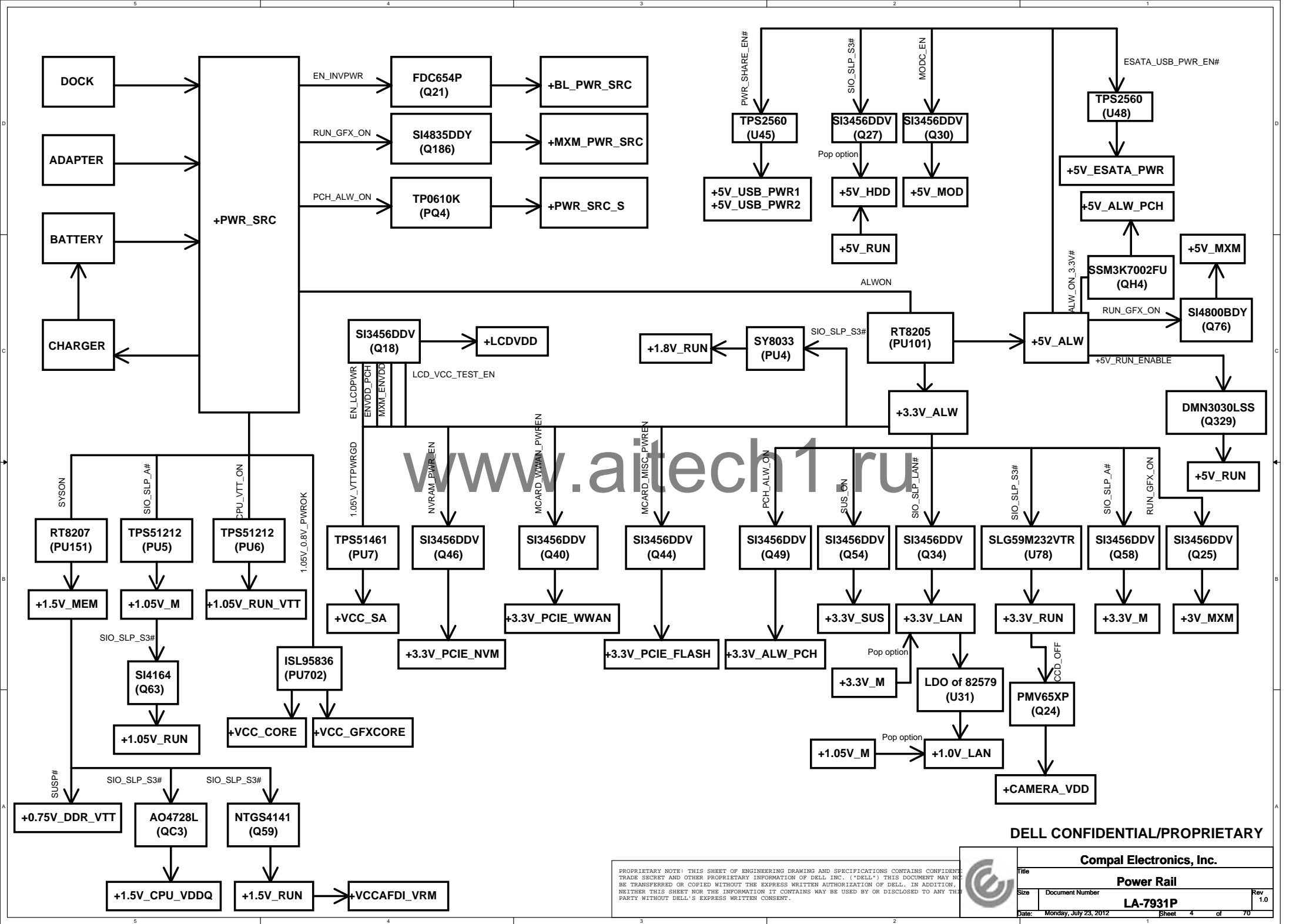
Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.50
			Add Plating		1.00
1	Top		Copper foil	0.5oz	0.65
			Prepreg	1080	2.60
2	GND1	3.7	Copper foil	1oz	1.35
			Core	4mil	3.91
3	Sig 1		Copper foil	1oz	1.35
			Prepreg	2116Mx2	8.26
4	GND/PWR	4.1	Copper foil	1oz	1.35
			Core	4mil	3.91
5	Sig 2	3.7	Copper foil	1oz	1.35
			Prepreg	1080Hx2	4.80
6	Sig 3	3.8	Copper foil	1oz	1.35
			Core	4mil	3.91
7	GND/PWR	3.7	Copper foil	1oz	1.35
			Prepreg	2116Mx2	8.26
8	Sig 4	4.1	Copper foil	1oz	1.35
			Core	4mil	3.91
9	GND 3	3.7	Copper foil	1oz	1.35
			Prepreg	1080	2.60
10	Bottom	3.7	Copper foil	0.5oz	0.65
			Add Plating		1.00
			SolderMask		0.50
Overall Thickness (1.45mm ± 10%)				57.09	57.26000 1.454404

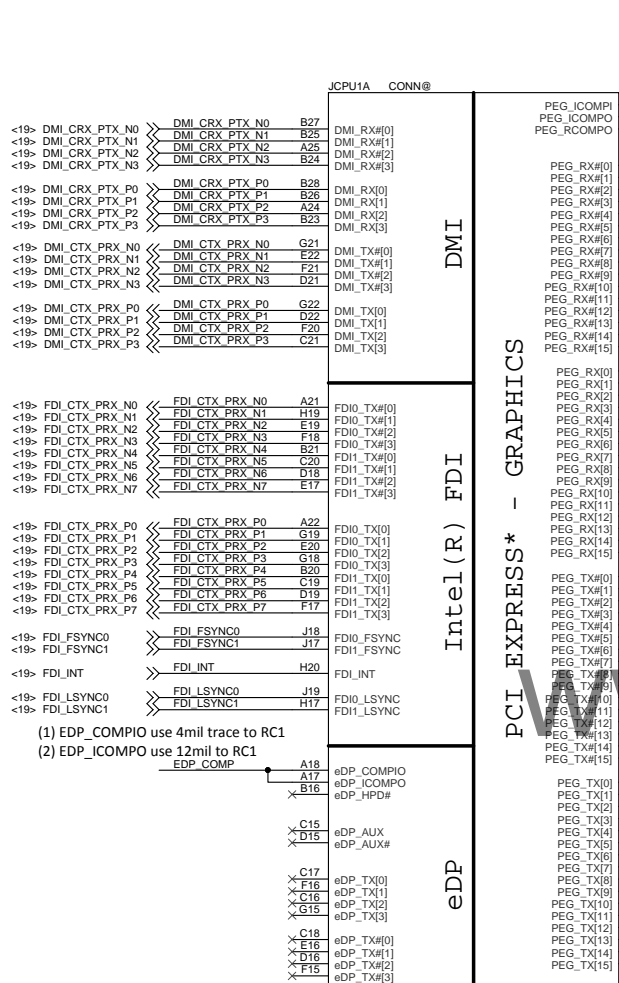
PCI EXPRESS	DESTINATION
Lane 1	NA
Lane 2	MINI CARD-1 WLAN/DMC
Lane 3	Express Card
Lane 4	NA
Lane 5	MINI CARD-3 (Pink Panther)
Lane 6	MINI CARD-2 WWAN/mSATA/GPS
Lane 7	10/100/1G LOM
Lane 8	Cardreader

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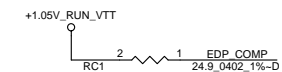
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Index and Config.			
Title	LA-7931P		
Size	Document Number	Rev	1.0
Date	Monday, July 23, 2012	Sheet	3 of 70

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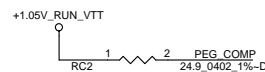


- (1) EDP_COMPIO use 4mil trace to RC1
(2) EDP_ICOMPO use 12mil to RC1



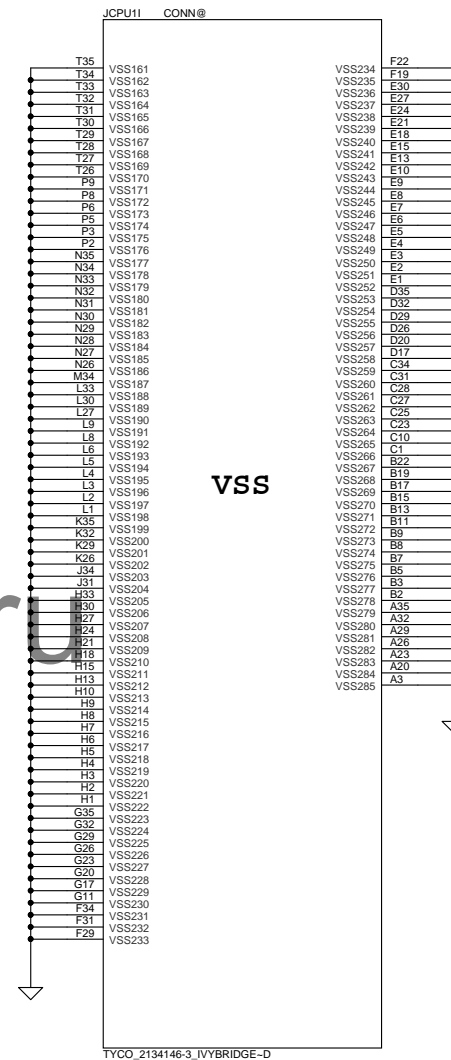
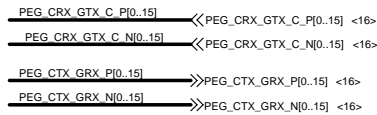
eDP Compensation

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



PEG Compensation

PEG_ICOMPI and RCOMPO signals should be shorted and routed with
- max length = 500 mils
- typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with
- max length = 500 mils
- typical impedance = 14.5 mohms



Link CIS OK
0722

Link CIS OK

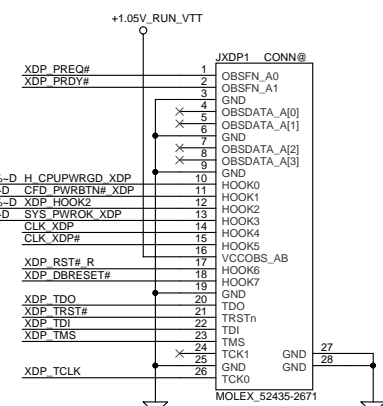
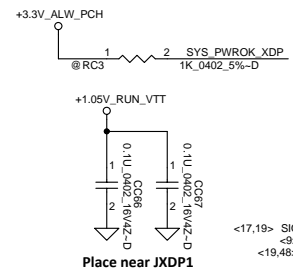
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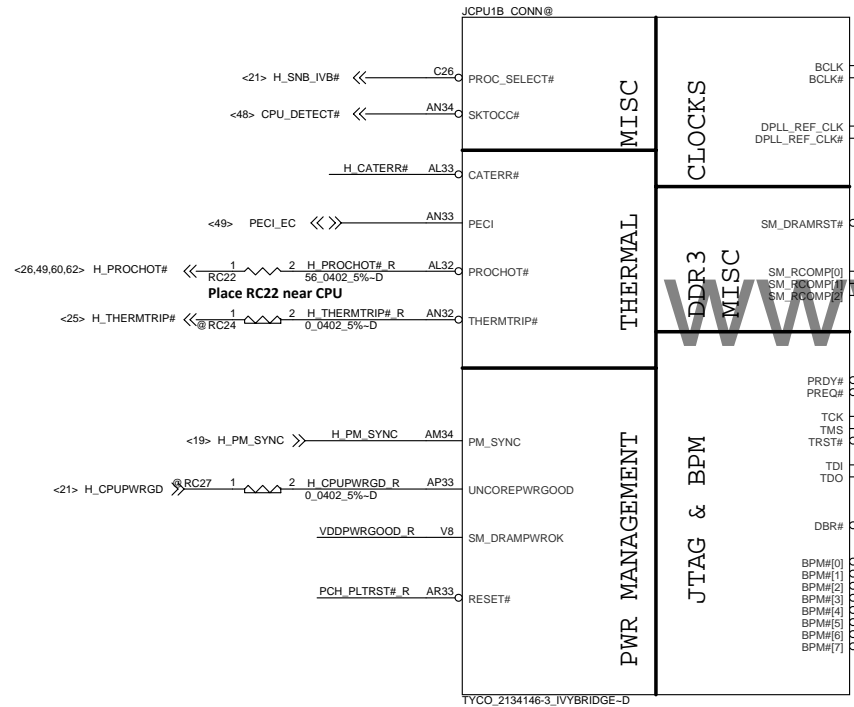


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Ivy Bridge (1/6)			
Size	Document Number		Rev
	LA-7931P		1.0
Date:	Monday, July 23, 2012		Sheet 6 of 70

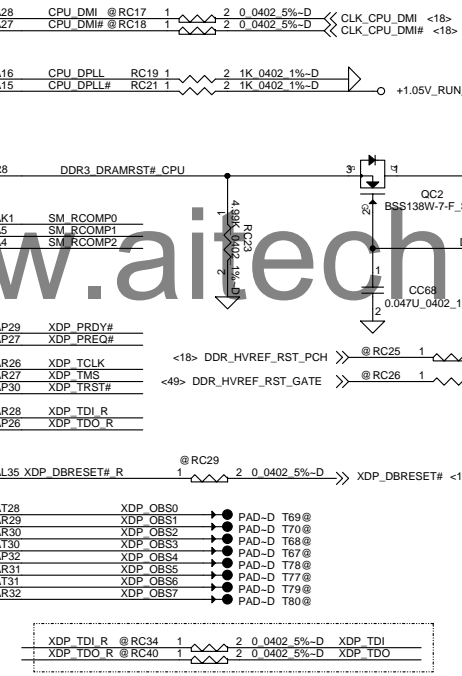
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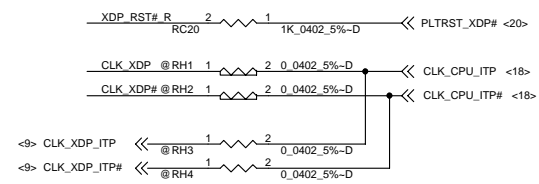
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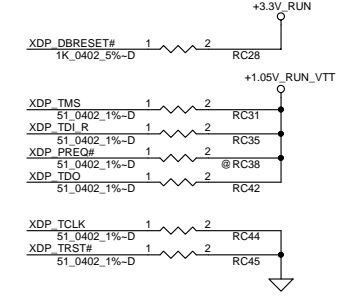
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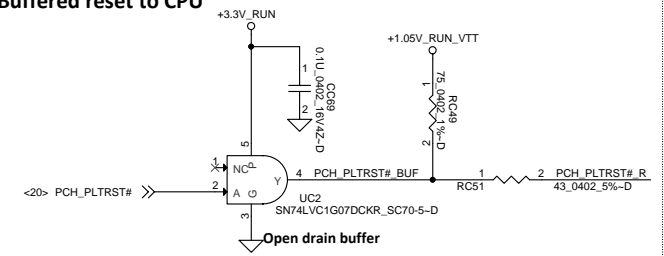
For ESD concern, please put near CPU



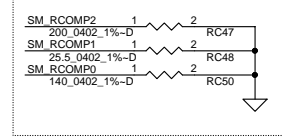
PU/PD for JTAG signals



Buffered reset to CPU



Max length = 500 mils
Trace width = 15mils

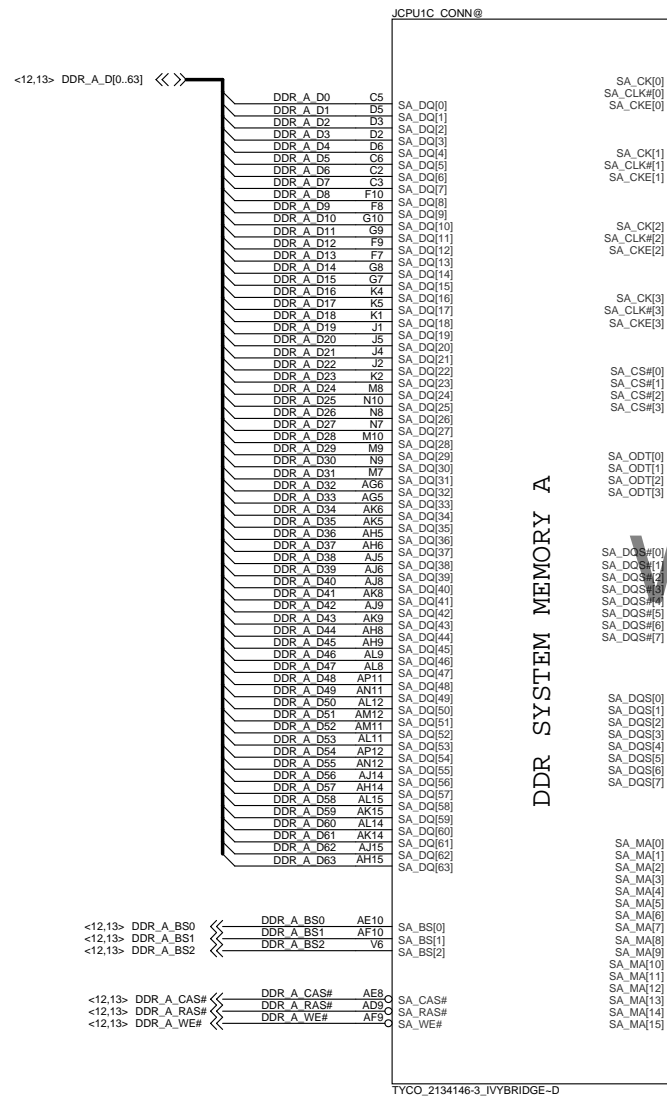


Avoid stub in the PWRGD path while placing resistors RC27& RC46

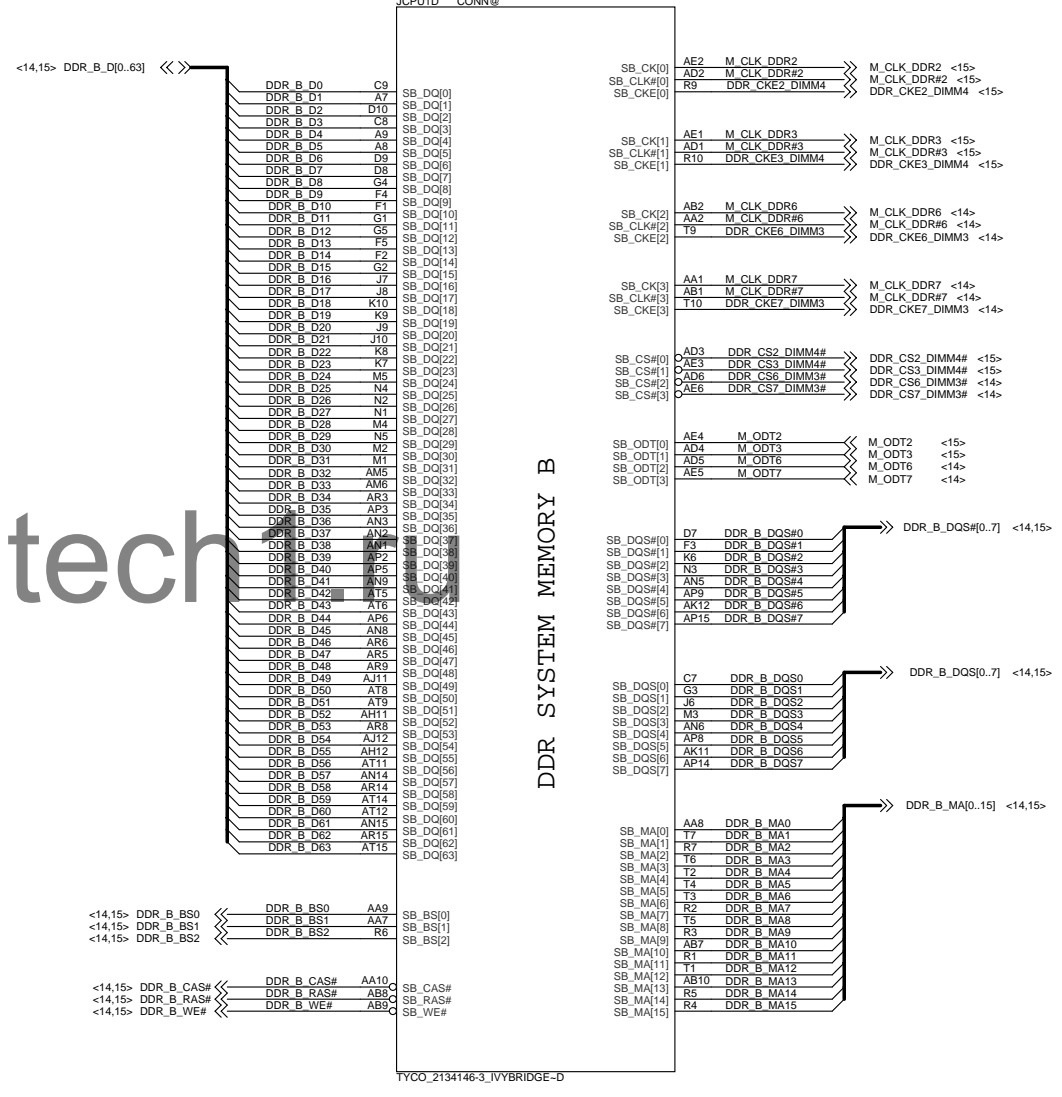
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Size	Document Number	LA-7931P	Rev
			1.0
Date:	Monday, July 23, 2012	Sheet	7 of 70

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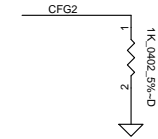
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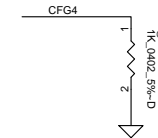
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Size	Document Number	Rev
	LA-7931P	1.0
Date	Monday, July 23, 2012	
Sheet	8	of 70

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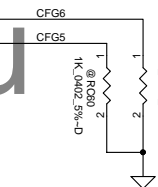
CFG Straps for Processor



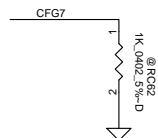
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



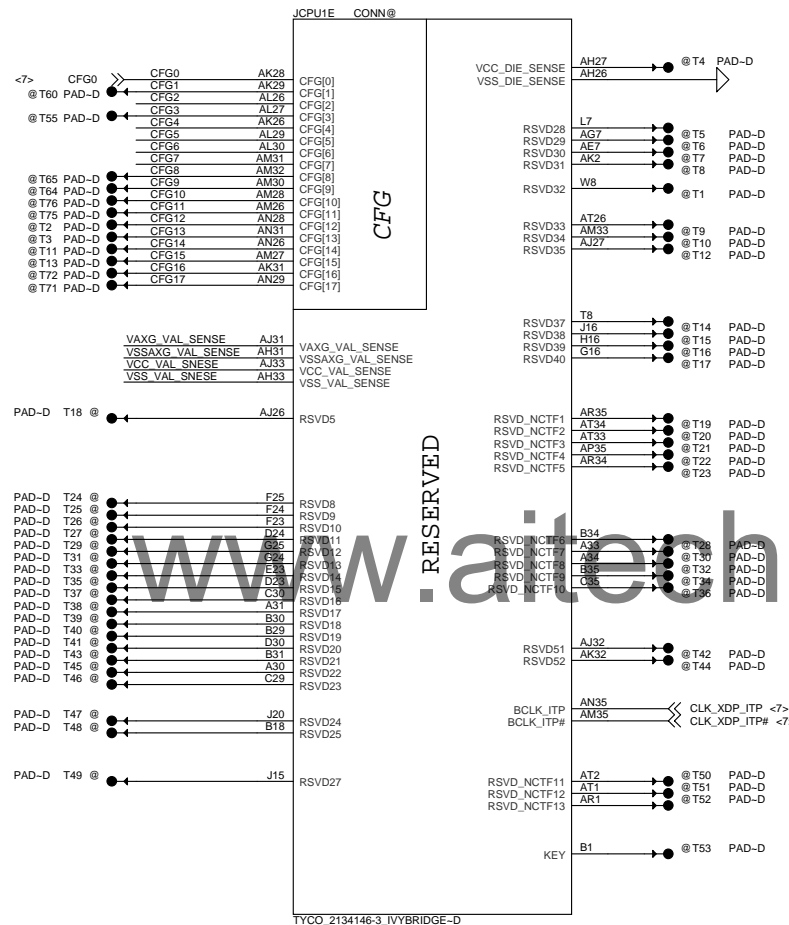
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled
	10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
	01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
	00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



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Size	Document Number	Rev	
	LA-7931P	1.0	
Date:	Monday, July 23, 2012	Sheet	9 of 70

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POWER

JCPU1F CONN@

+VCC_CORE
97A

- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AF26 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC35 VCC31
- AC34 VCC32
- AC33 VCC33
- AC32 VCC34
- AC31 VCC35
- AC30 VCC36
- AC29 VCC37
- AC28 VCC38
- AC27 VCC39
- AC26 VCC40
- AA35 VCC41
- AA34 VCC42
- AA33 VCC43
- AA32 VCC44
- AA31 VCC45
- AA30 VCC46
- AA29 VCC47
- AA28 VCC48
- AA27 VCC49
- AA26 VCC50
- Y35 VCC51
- Y34 VCC52
- Y33 VCC53
- Y32 VCC54
- Y31 VCC55
- Y30 VCC56
- Y29 VCC57
- Y28 VCC58
- Y27 VCC59
- Y26 VCC60
- V35 VCC61
- V34 VCC62
- V33 VCC63
- V32 VCC64
- V31 VCC65
- V30 VCC66
- V29 VCC67
- V28 VCC68
- V27 VCC69
- V26 VCC70
- U35 VCC71
- U34 VCC72
- U33 VCC73
- U32 VCC74
- U31 VCC75
- U30 VCC76
- U29 VCC77
- U28 VCC78
- U27 VCC79
- U26 VCC80
- R35 VCC81
- R34 VCC82
- R33 VCC83
- R32 VCC84
- R31 VCC85
- R30 VCC86
- R29 VCC87
- R28 VCC88
- R27 VCC89
- R26 VCC90
- P35 VCC91
- P34 VCC92
- P33 VCC93
- P32 VCC94
- P31 VCC95
- P30 VCC96
- P29 VCC97
- P28 VCC98
- P27 VCC99
- P26 VCC100

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

TYCO_2134146-3_IVYBRIDGE-D

Link CIS OK

+1.05V_RUN_VTT

8.5A

- VCCIO1 AH13
- VCCIO2 AH10
- VCCIO3 AG10
- VCCIO4 Y10
- VCCIO5 U10
- VCCIO6 P10
- VCCIO7 L10
- VCCIO8 J14
- VCCIO9 J13
- VCCIO10 J12
- VCCIO11 J11
- VCCIO12 H12
- VCCIO13 H11
- VCCIO14 G14
- VCCIO15 G13
- VCCIO16 G12
- VCCIO17 F14
- VCCIO18 F13
- VCCIO19 F12
- VCCIO20 F11
- VCCIO21 E14
- VCCIO22 E13
- VCCIO23 E12
- VCCIO24 E11
- VCCIO25 D14
- VCCIO26 D13
- VCCIO27 D12
- VCCIO28 D11
- VCCIO29 C14
- VCCIO30 C13
- VCCIO31 C12
- VCCIO32 C11
- VCCIO33 B14
- VCCIO34 B12
- VCCIO35 A14
- VCCIO36 A13
- VCCIO37 A12
- VCCIO38 A11
- VCCIO39 J23
- VCCIO40 J23

Note: Place the PU resistors close to CPU
RC63 close to CPU 300 - 1500mils

H CPU_SVIDALRT# RC64 1 2 43.0402 5%-D <<VIDALERT_N <60>

+1.05V_RUN_VTT

CAD Note: Place the PU resistors close to CPU
RC65 close to CPU 300 - 1500mils

VIDALERT# H CPU_SVIDALRT# RC65 1 2 130.0402 1%-D <60> <<VIDSOUT <60>

VCC_SENSE VSS_SENSE VCCIO_SENSE VSS_SENSE_VCCIO Place RC68, RC69 near CPU @ RC66 1 2 100.0402 1%-D RC67 1 2 100.0402 1%-D RC70 1 2 10.0402 1%-D RC71 1 2 100.0402 1%-D RC72 1 2 10.0402 1%-D VCCSENSE <60> VSSSENSE <60> VTT_SENSE <58> VSSIO_SENSE_R <58>

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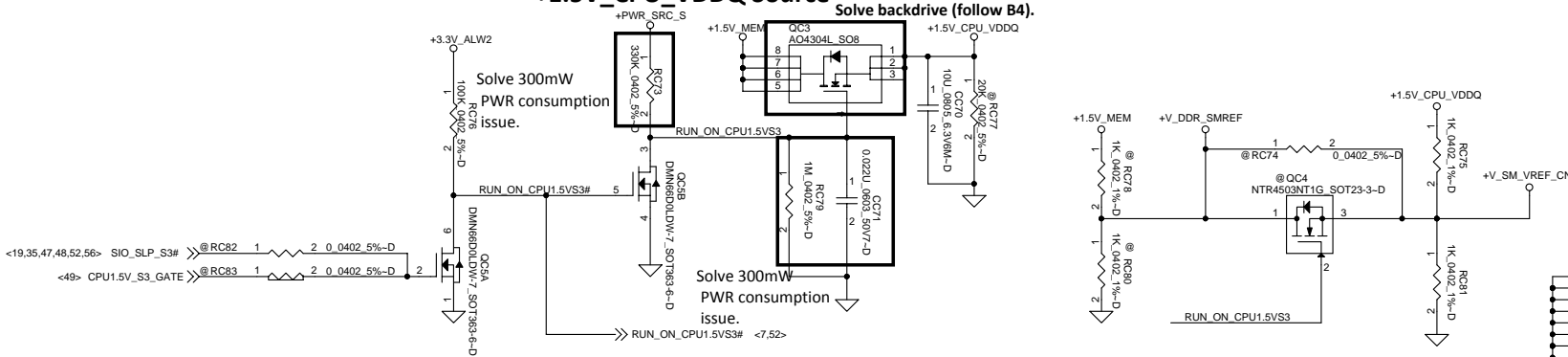
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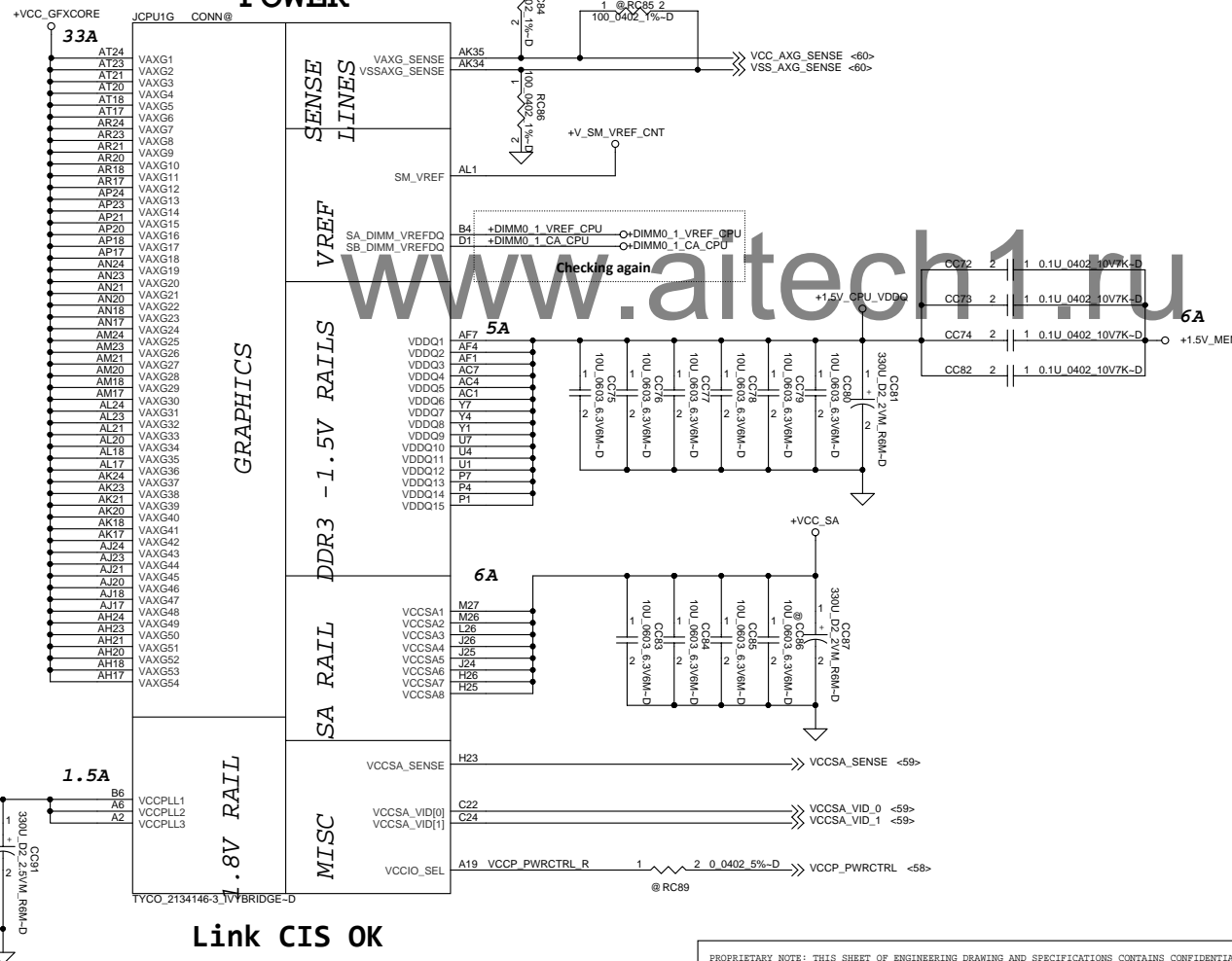
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Size	Document Number	Rev	
	LA-7931P	1.0	
Date	Monday, July 23, 2012	Sheet	10 of 70

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+1.5V_CPU_VDDQ Source
+PWR_SRC S Solve backdrive (follow B4).



POWER



JCPU11H_CONN@		
AT35	VSS1	VSS81
AT32	VSS2	VSS82
AT29	VSS3	VSS83
AT27	VSS4	VSS84
AT25	VSS5	VSS85
AT22	VSS6	VSS86
AT19	VSS7	VSS87
AT16	VSS8	VSS88
AT13	VSS9	VSS89
AT10	VSS10	VSS90
AT7	VSS11	VSS91
AT3	VSS12	VSS92
AR25	VSS13	VSS93
AR22	VSS14	VSS94
AR19	VSS15	VSS95
AR16	VSS16	VSS96
AR13	VSS17	VSS98
AR10	VSS18	VSS99
AR7	VSS19	VSS100
AR4	VSS20	VSS101
AR2	VSS21	VSS102
AP34	VSS22	VSS103
AP31	VSS23	VSS104
AP28	VSS24	VSS105
AP25	VSS25	VSS106
AP22	VSS26	VSS107
AP19	VSS27	VSS108
AP16	VSS28	VSS109
AP13	VSS29	VSS110
AP10	VSS30	VSS111
AP7	VSS31	VSS112
AP4	VSS32	VSS113
AP1	VSS33	VSS114
AN30	VSS34	VSS115
AN27	VSS35	VSS116
AN25	VSS36	VSS117
AN22	VSS37	VSS118
AN19	VSS38	VSS119
AN16	VSS39	VSS120
AN13	VSS40	VSS121
AN10	VSS41	VSS122
AN7	VSS42	VSS123
AN4	VSS43	VSS124
AN1	VSS44	VSS125
AM29	VSS45	VSS126
AM25	VSS46	VSS127
AM22	VSS47	VSS128
AM19	VSS48	VSS129
AM16	VSS49	VSS130
AM13	VSS50	VSS131
AM10	VSS51	VSS132
AM7	VSS52	VSS133
AM4	VSS53	VSS134
AM2	VSS54	VSS135
AM1	VSS55	VSS136
AL34	VSS56	VSS137
AL31	VSS57	VSS138
AL28	VSS58	VSS139
AL25	VSS59	VSS140
AL22	VSS60	VSS141
AL19	VSS61	VSS142
AL16	VSS62	VSS143
AL13	VSS63	VSS144
AL10	VSS64	VSS145
AL7	VSS65	VSS146
AL4	VSS66	VSS147
AL2	VSS67	VSS148
AK33	VSS68	VSS149
AK30	VSS69	VSS150
AK27	VSS70	VSS151
AK25	VSS71	VSS152
AK22	VSS72	VSS153
AK19	VSS73	VSS154
AK16	VSS74	VSS155
AK13	VSS75	VSS156
AK10	VSS76	VSS157
AK7	VSS77	VSS158
AK4	VSS78	VSS159
AJ25	VSS79	VSS160
AJ28	VSS80	

Link CIS OK

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Ivy Bridge (6/6)

LA-7931P

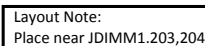
Rev	1.0
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Date: Monday, July 23, 2012

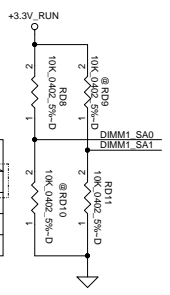
Sheet 11 of 70

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Populate RD1 for Intel DDR3 VREFDQ multiple methods M1



SA0	SA1	
1	0	DIMM1
0	0	DIMM2
1	1	DIMM3
0	1	DIMM4



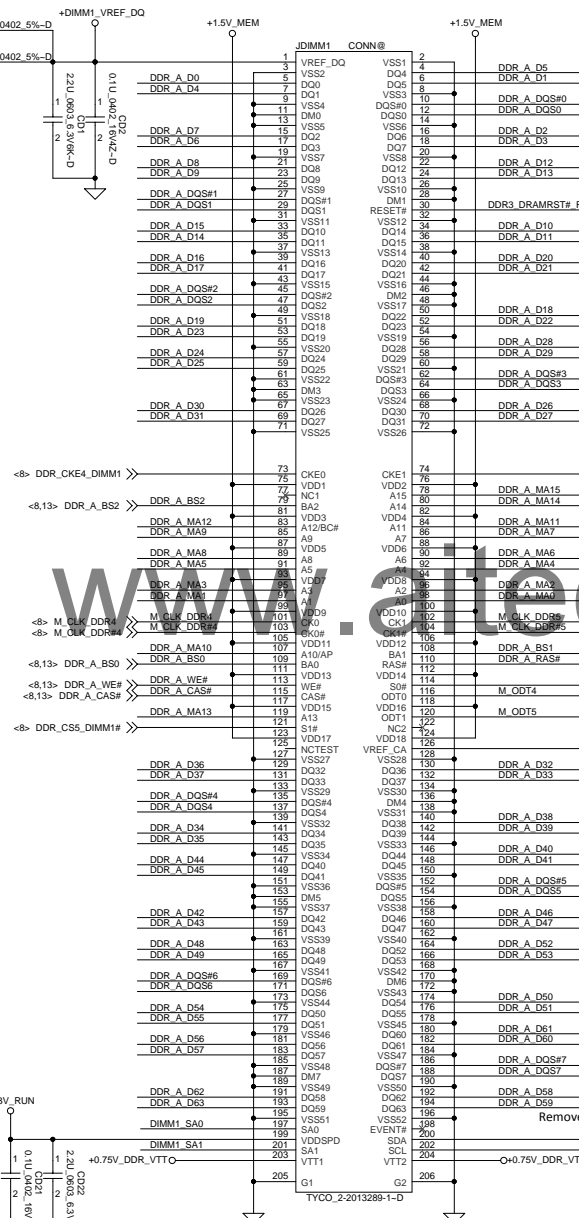
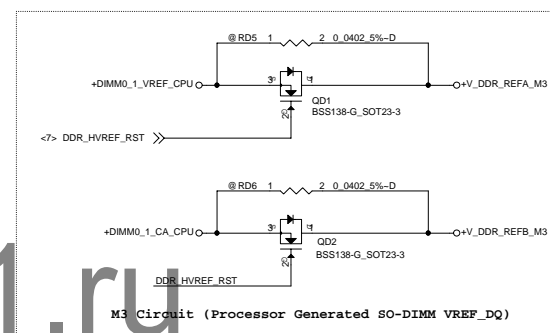
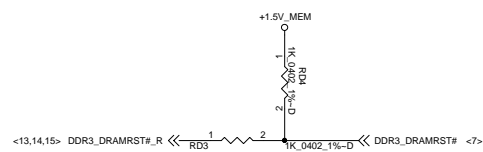
JDIMM3 (Ch B1 H=9.2 STD)

JDIMM1 (Ch A1 H=5.2 STD)

CPU

BOT

JDIMM2 (Ch A0 H=5.2 REV) JDIMM4 (Ch B0 H=5.2 STD)



Remove 0 ohm, due to layout space limitation.

			DDR_XDP_WAN_SMBDATA	<13,14,15,17,18,35,43>
			DDR_XDP_WAN_SMBCLK	<13,14,15,17,18,35,43>

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0722

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DDRIII-SODIMM SLOT1

LA-7931P

Re

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All VREF traces should have 10 mil trace width

<8,12> DDR_A_DQS#[0..7] <<
<8,12> DDR_A_D[0..63] <<
<8,12> DDR_A_DQS#[0..7] <<
<8,12> DDR_A_MA[0..15] <<

JDIMM2 REV Type H=5.2

JDIMM3 (Ch B1 H=9.2 STD)

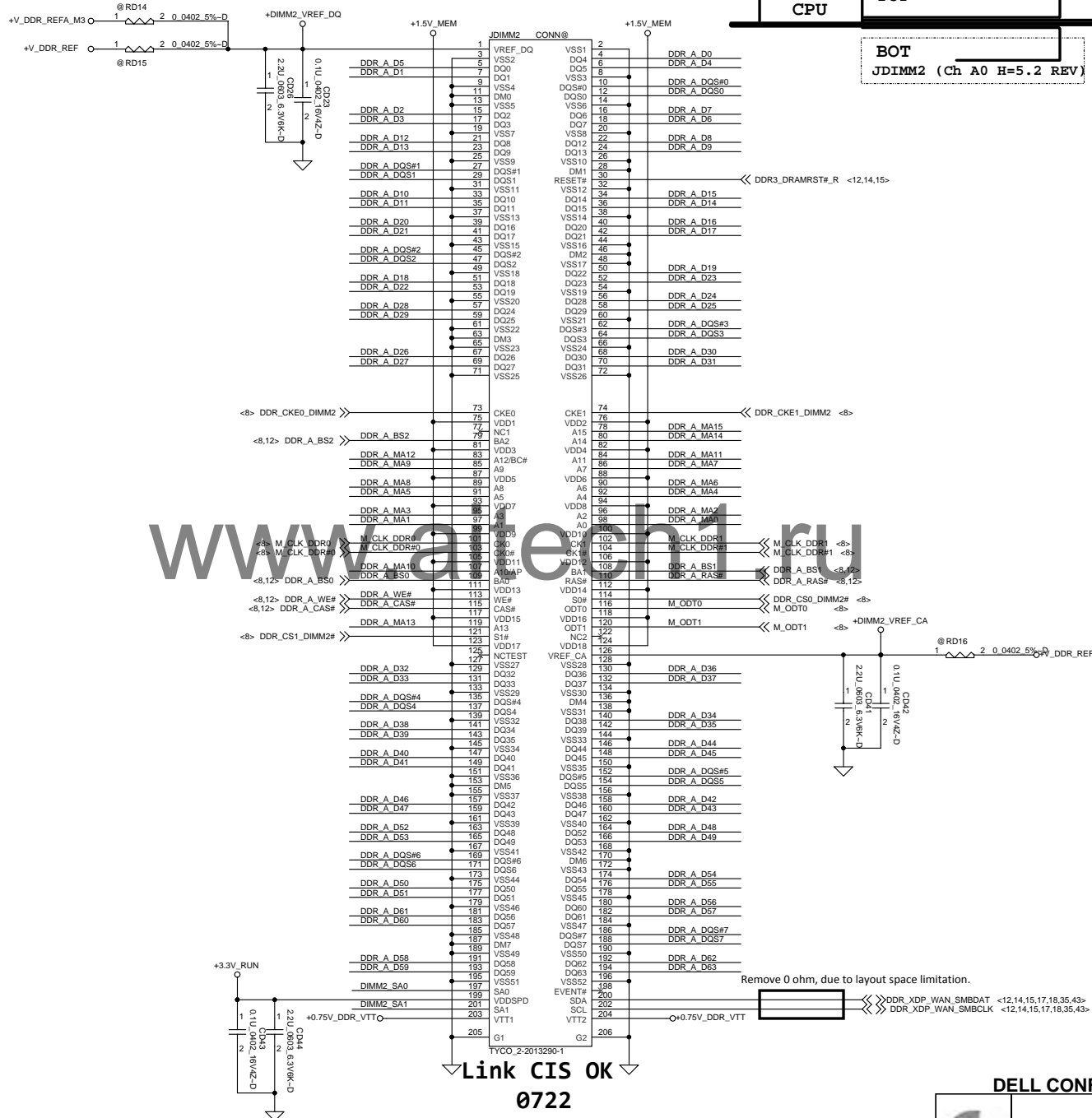
JDIMM1 (Ch A1 H=5.2 STD)

BOT
JDIMM2 (Ch A0 H=5.2 REV)

JDIMM4 (Ch B0 H=5.2 STD)

CPU

TOP



Layout Note:
Place near JDIMM3.Pin 203,204

DIMM Select

SA0	SA1	
1	0	DIMM1
0	0	DIMM2
1	1	DIMM3
0	1	DIMM4

Link CIS OK
0722

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DDR3-SODIMM SLOT2

LA-7931P

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Sheet 13 of 70

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JDIMM3 STD Type H=9.2

JDIMM3 (Ch B1 H=9.2 STD)

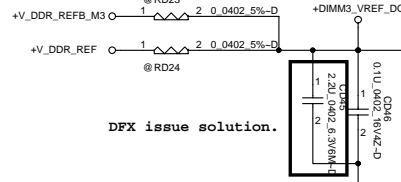
JDIMM1 (Ch A1 H=5.2 STD)

CPU

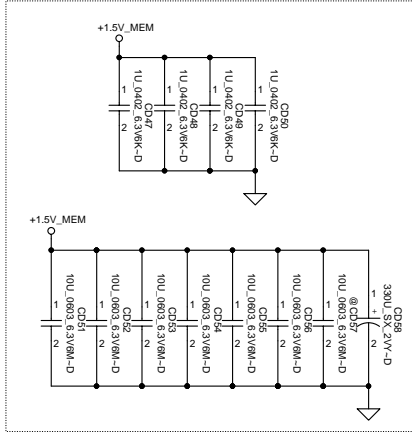
TOP

BOT

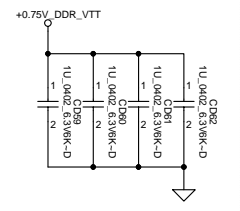
JDIMM2 (Ch A0 H=5.2 REV) JDIMM4 (Ch B0 H=5.2 STD)



All VREF traces should have 10 mil trace width

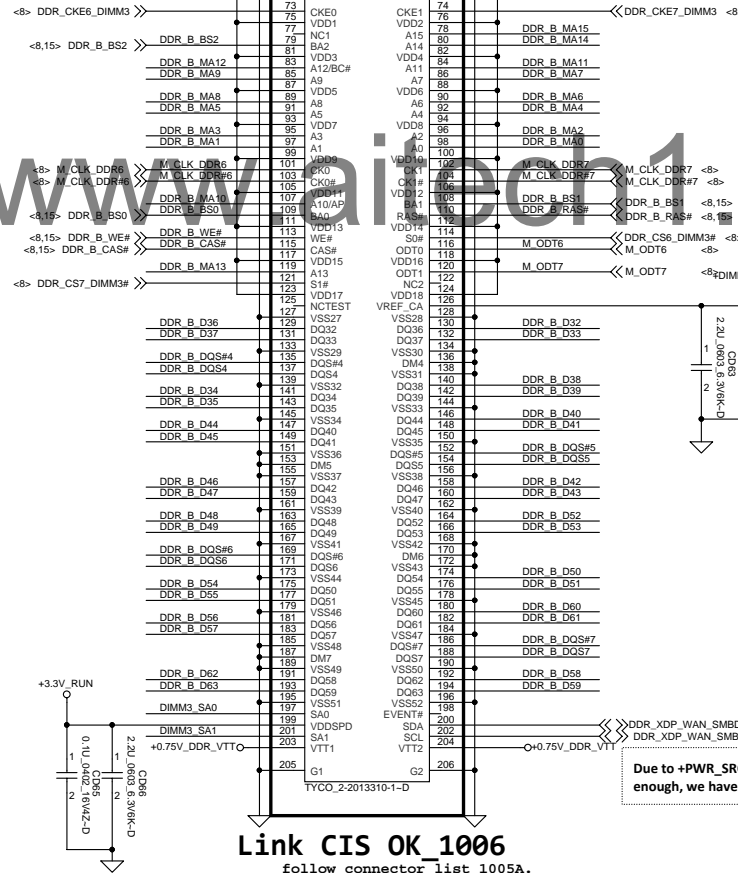


Layout Note:
Place near JDIMM3.Pin 203,204



DIMM Select

SA0	SA1	
1	0	DIMM1
0	0	DIMM2
1	1	DIMM3
0	1	DIMM4



Due to +PWR_SRC trace width nearby H16 wasn't enough, we have to increase it so remove RD30 & RD31.

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DDR3-SODIMM SLOT3

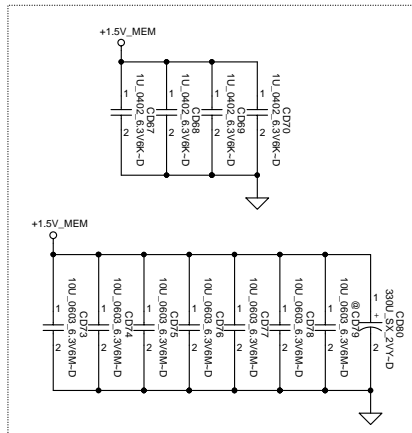
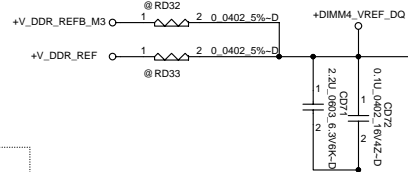
LA-7931P

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Sheet 14 of 70

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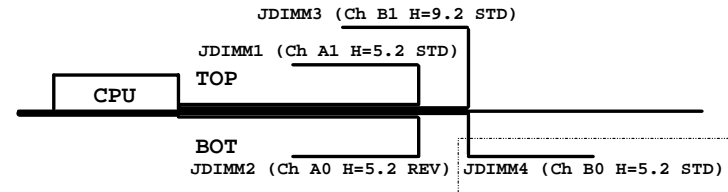
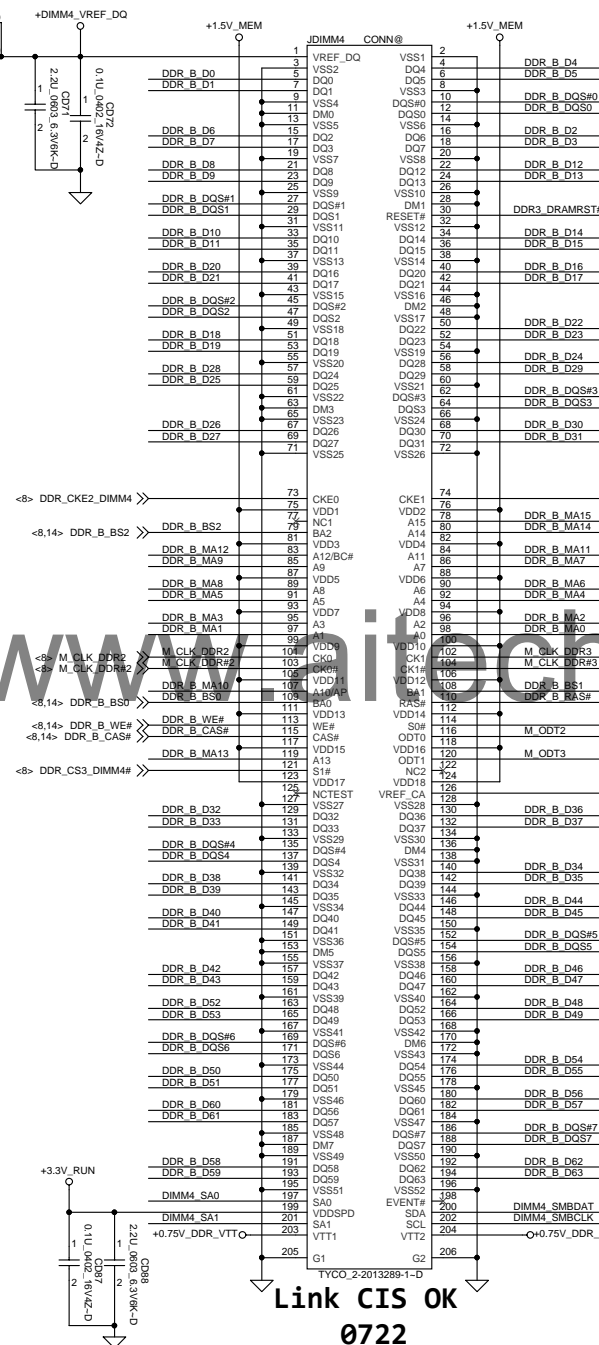
```
<8,14> DDR_B_DQS#[0..7] <<>>
<8,14> DDR_B_D[0..63] <<>>
<8,14> DDR_B_DQS[0..7] <<>>
<8,14> DDR_B_MA[0..15] >>>>
```



The diagram illustrates a power plane for a DDR2 memory bank. A +0.75V DDR_VTT supply is connected to a series of four capacitors (CD81, CD82, CD83, CD94) connected in parallel to ground. Each capacitor is labeled with its value: 1u0402, 6.3V6K-D.

SA0	SA1	
1	0	DIMM1
0	0	DIMM2
1	1	DIMM3
0	1	DIMM4

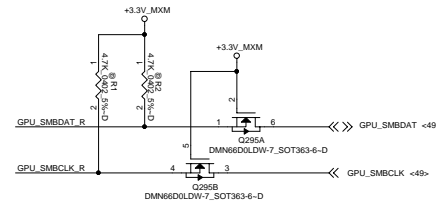
Figure 10-10. DDR3 SDRAM pin connections (continued)



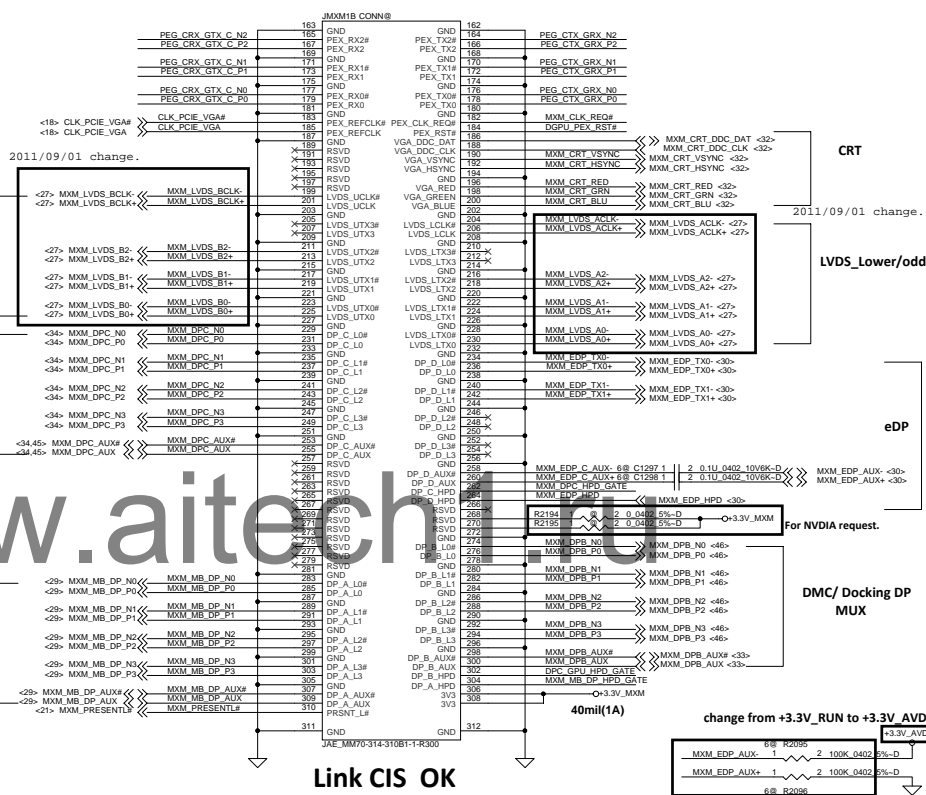
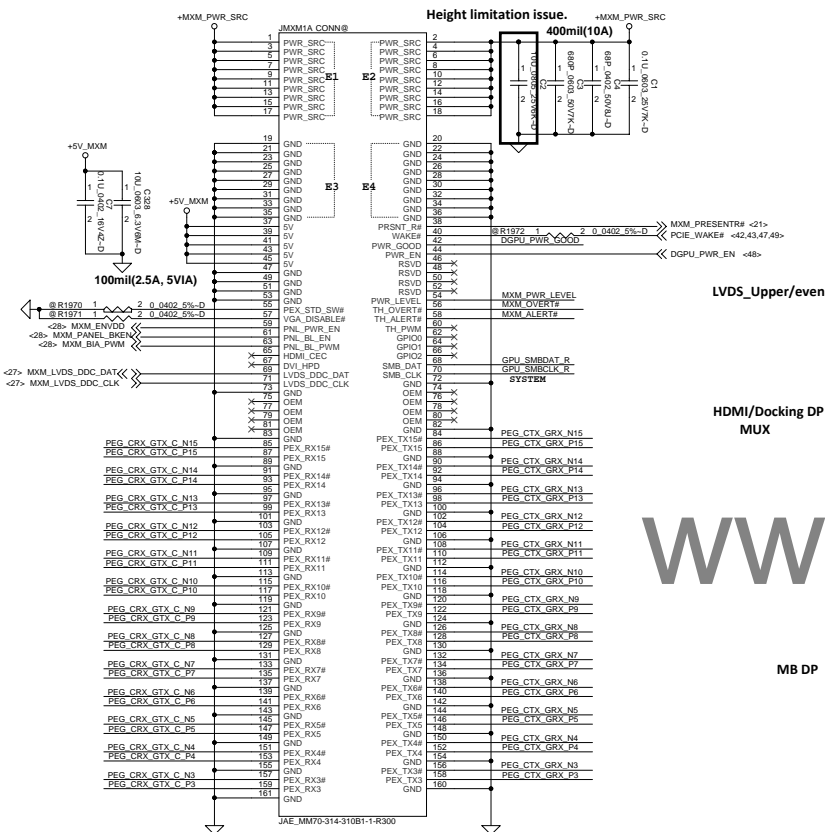
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Sheet 15 of 70

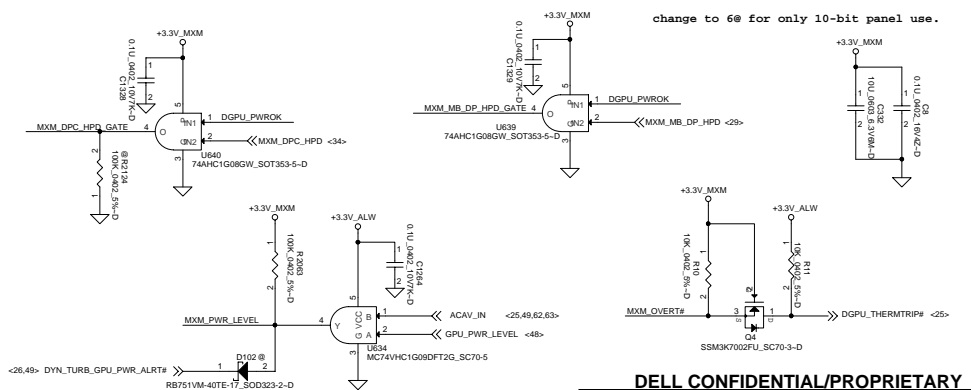
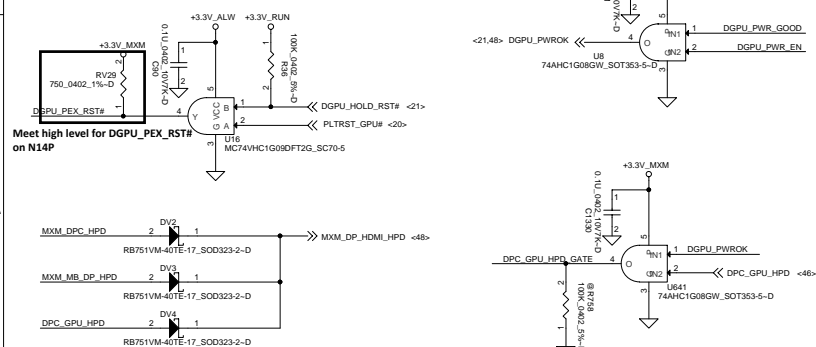
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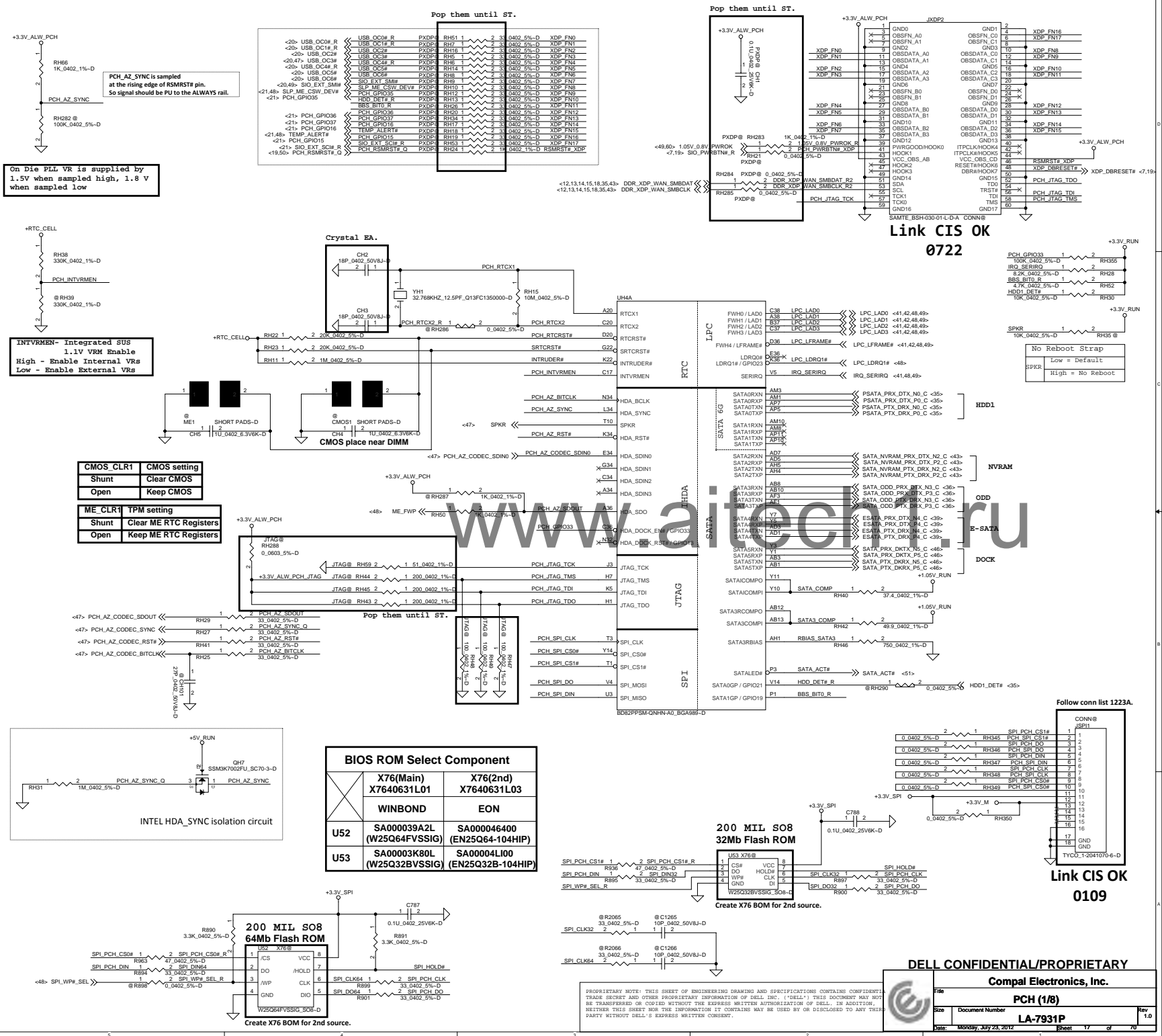


Height limitation issue.



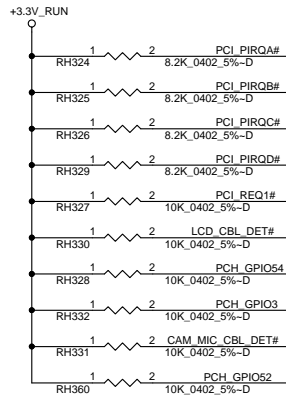
Link CIS OK
0722





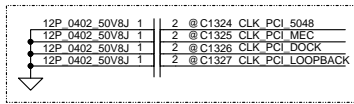
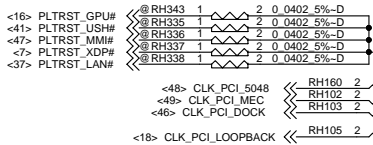
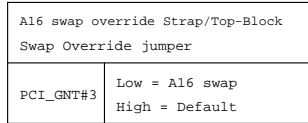
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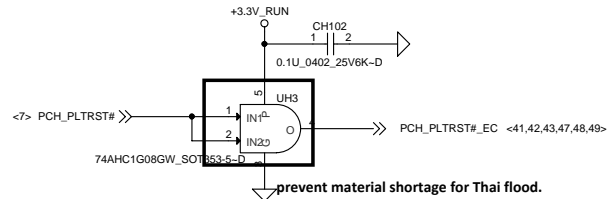


PCI_GNT3#

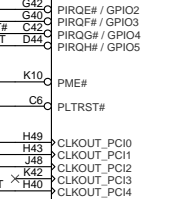
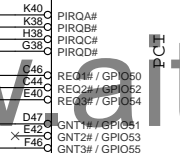
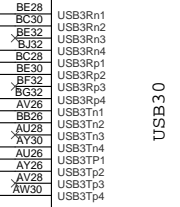
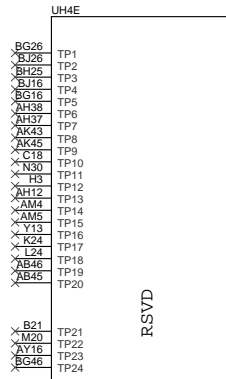
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100



For RF layout request



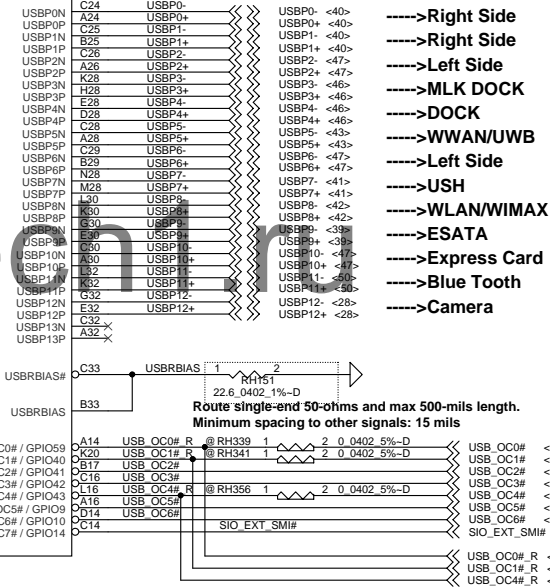
prevent material shortage for Thai flood.



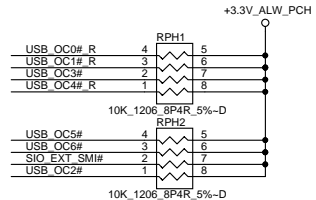
BD82PP5M-QNH-A0_BGA989-D

Boot BIOS Strap			
BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location	
0	0	LPC	
0	1	Reserved (NAND)	
1	0	PCI	
1	1	SPI	

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- >Right Side
- >Right Side
- >Left Side
- >MLK DOCK
- >DOCK
- >WWAN/UWB
- >Left Side
- >USH
- >WLAN/WIMAX
- >ESATA
- >Express Card
- >Blue Tooth
- >Camera



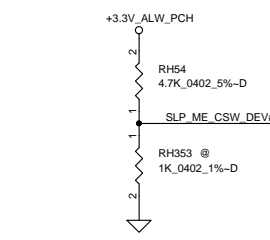
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PCH (4/8)

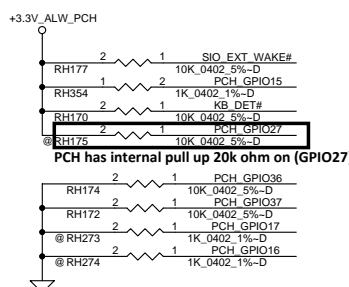
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Title			
Size	Document Number	Rev 1.0	
Date	Monday, July 23, 2012	Sheet	20 of 70

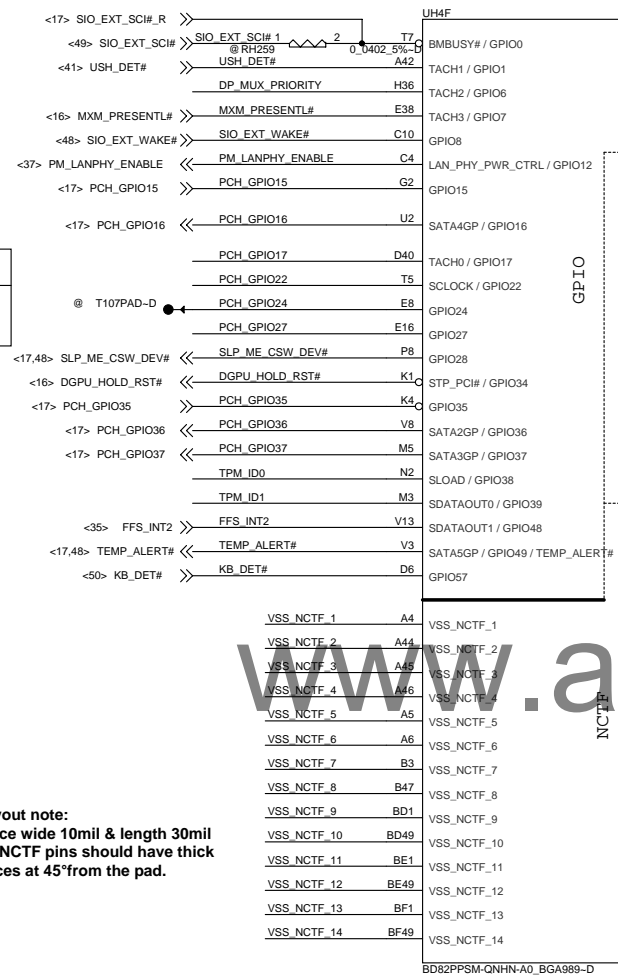


Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)

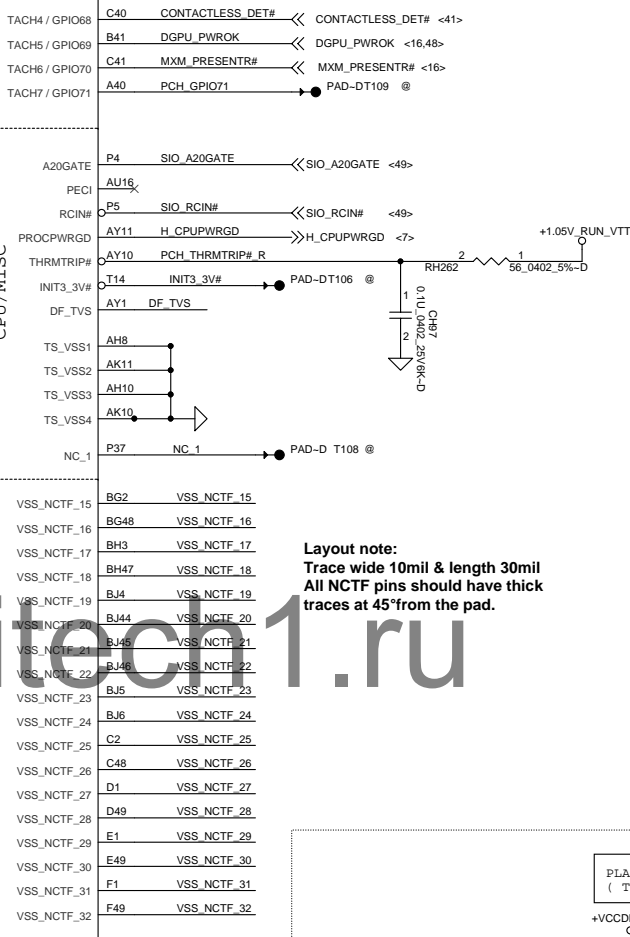
SLP_ME_CSW_DEV#	PLL ON DIE VR ENABLE
ENABLED - HIGH DEFAULT	
DISABLED - LOW	



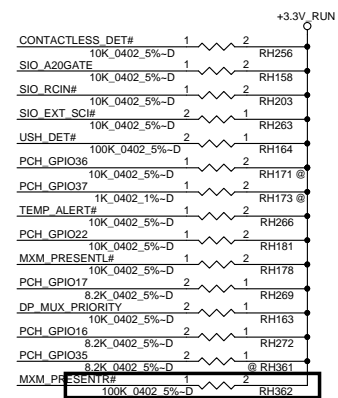
Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



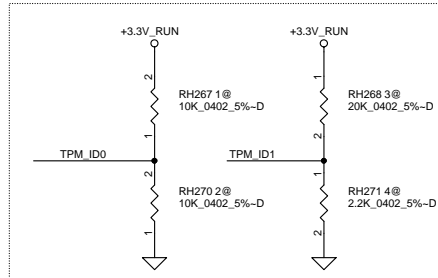
CPU / MISC
GPIO
NCTF



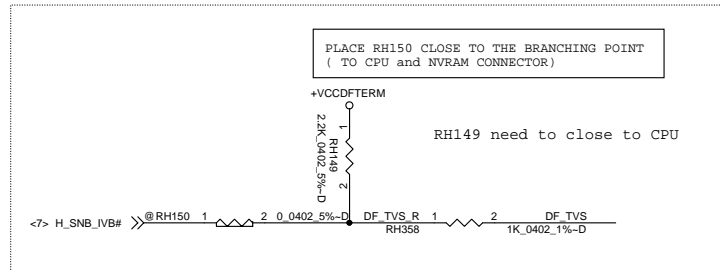
Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



power Saving.



	TPM_ID0	TPM_ID1
TCM	0	0
No TPM, No TCM	0	1
TBD		
TPM	1	1



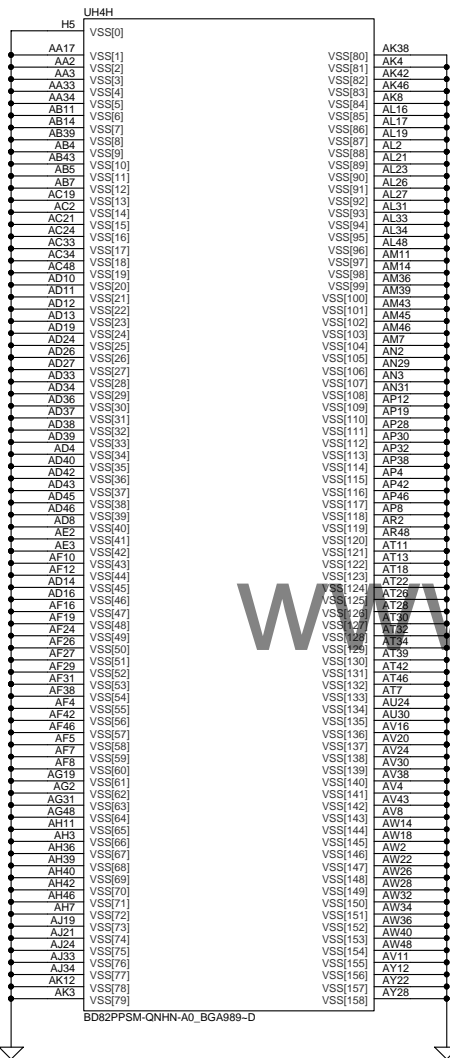
DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH

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PCH (5/8)			
Title	LA-7931P		
Size	Document Number	Rev 1.0	
Date	Monday, July 23, 2012	Sheet	21 of 70

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BD82PPSM-QNHN-A0_BGA989-D



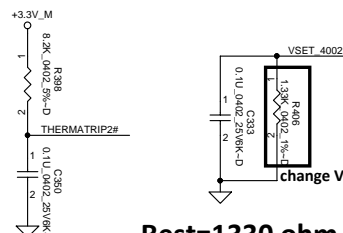
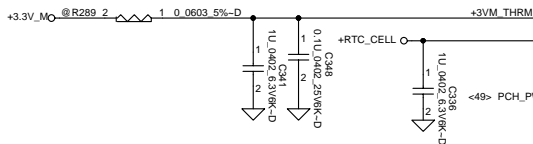
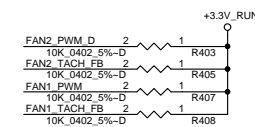
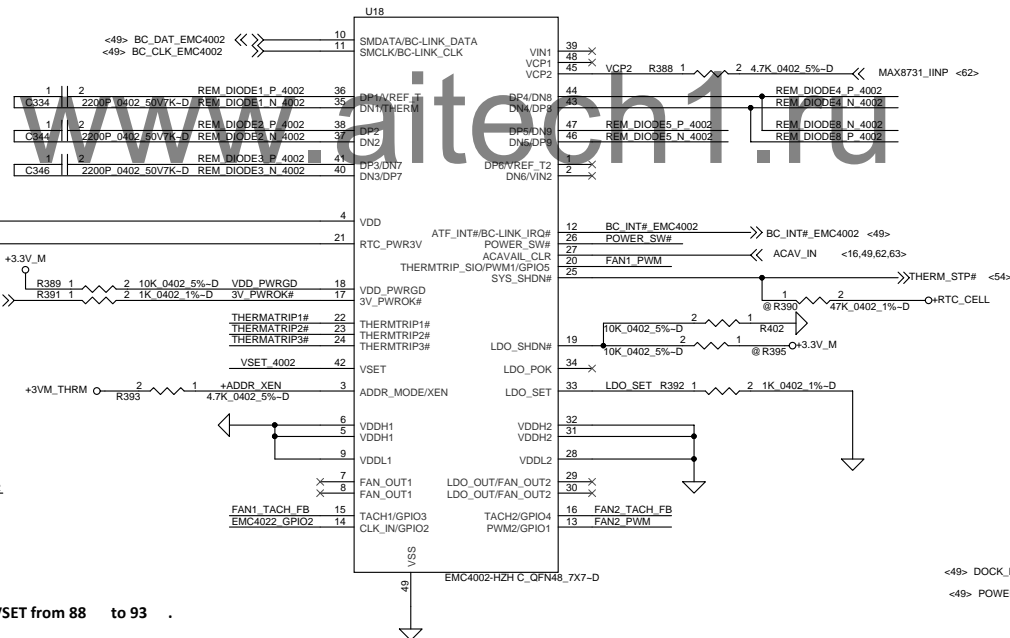
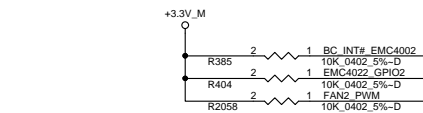
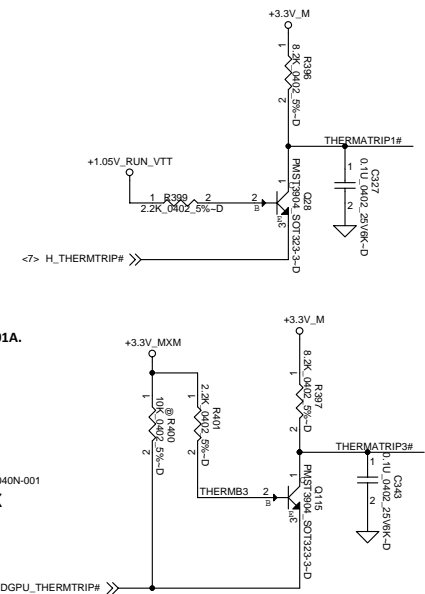
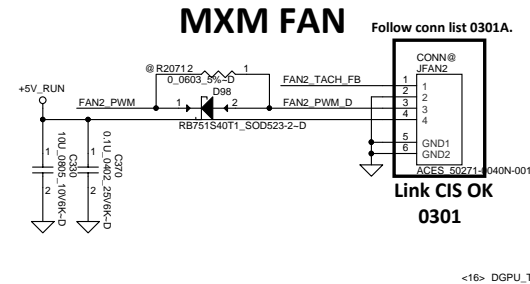
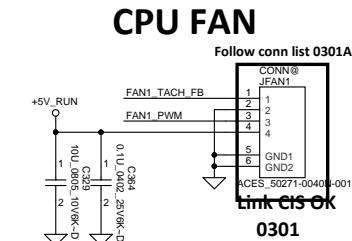
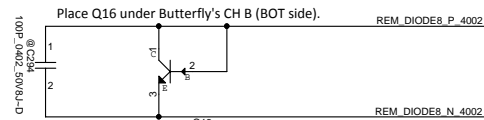
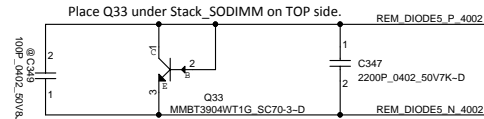
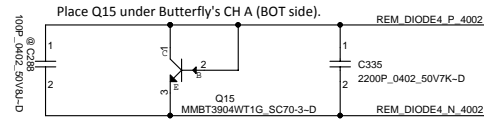
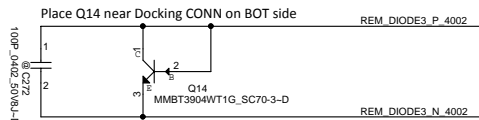
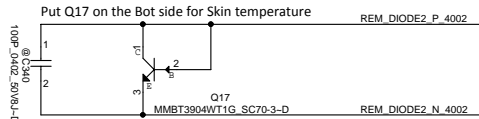
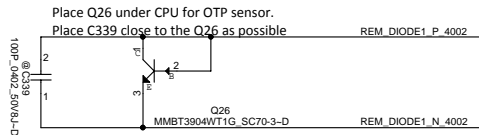
BD82PPSM-QNHN-A0_BGA989-D

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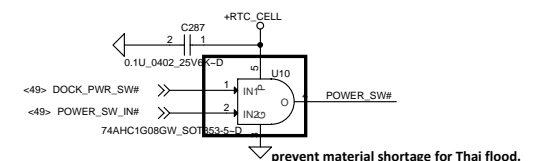
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Date	Monday, July 23, 2012	Sheet 24 of 70

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Rest=1330 ohm, Tp=93 degree



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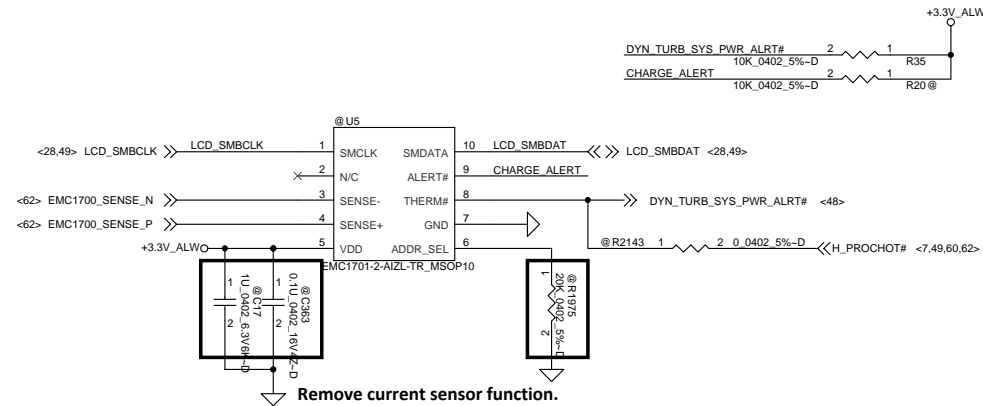
FAN control

File	Document Number	Rev
LA-7931P	1.0	
Date: Monday, July 23, 2012	Sheet 25 of 70	

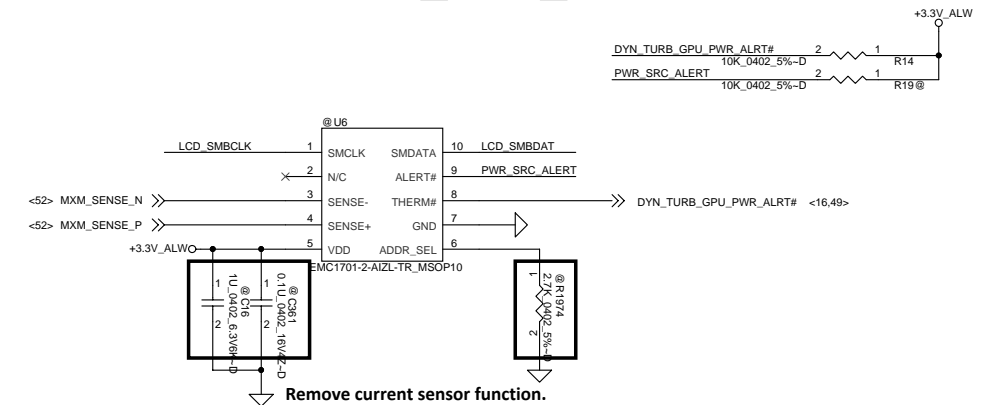
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Monitor Charger current

RESISTOR (5%)	SMBUS ADDRESS
0	1001_100(r/w)
100	1001_101(r/w)
180	1001_110(r/w)
300	1001_111(r/w)
430	1001_000(r/w)
560	1001_001(r/w)
750	1001_010(r/w)
1270	1001_011(r/w)
1600	0101_000(r/w)
2000	0101_001(r/w)
2700	0101_010(r/w)
3600	0101_011(r/w)
5600	0101_100(r/w)
9100	0101_100(r/w)
20000	0101_101(r/w)
Open	0011_000(r/w)



Monitor PWR_SRC_MXM



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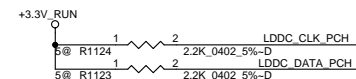
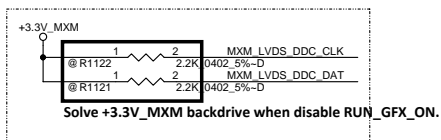
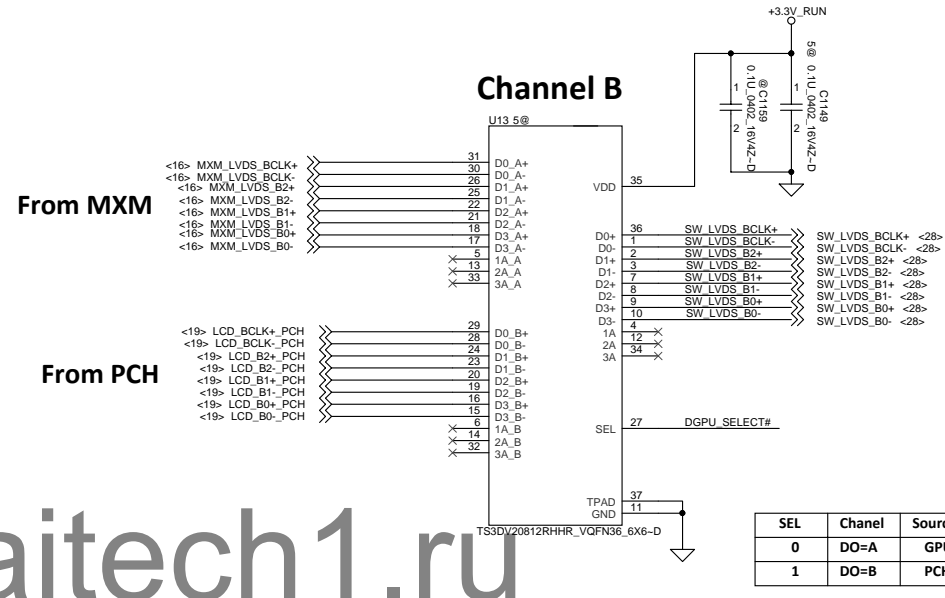
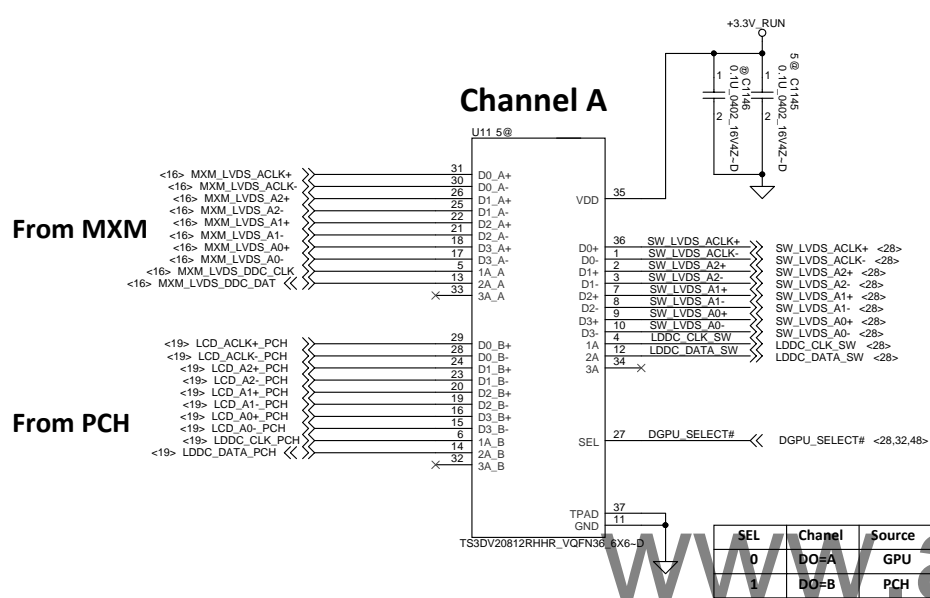


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Current Sensor

LA-7931P

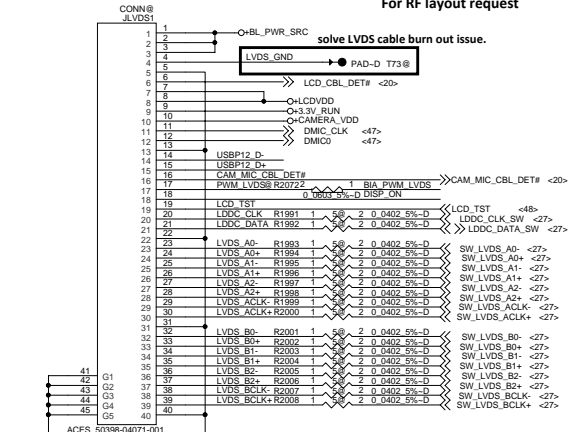
Size Document Number Rev 1.0
Date: Monday, July 23, 2012 Sheet 28 of 70



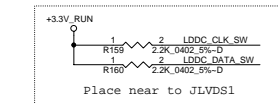
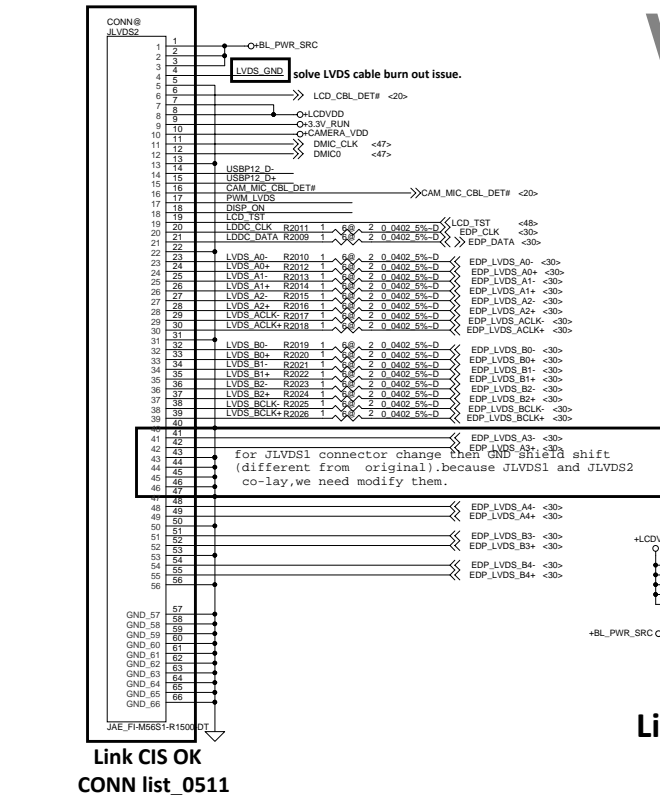
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Compal Electronics, Inc.			
Title LVDS SW			
Size	Document Number LA-7931P	Rev 1.0	
Date Monday, July 23, 2012	Sheet 27	of 70	

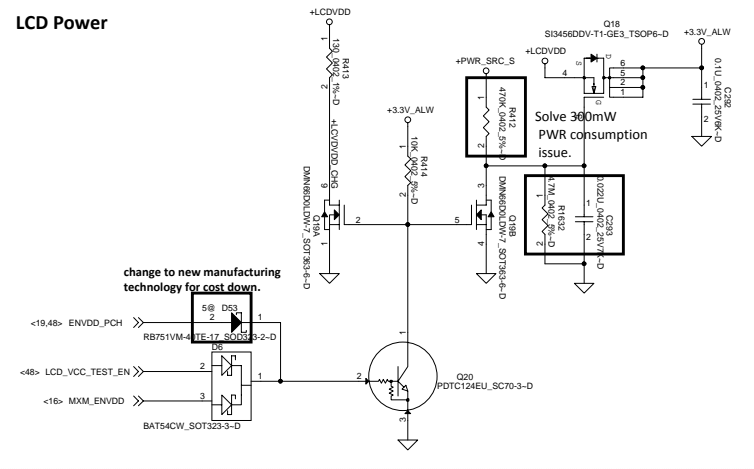
For 6-bit LCD panel



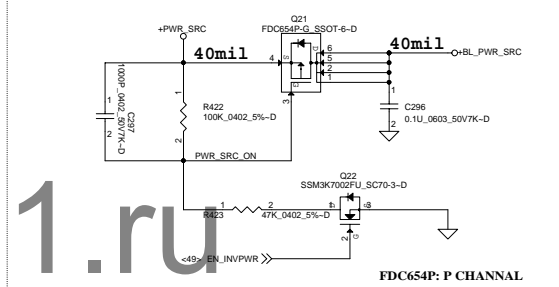
For 10-bit LCD panel



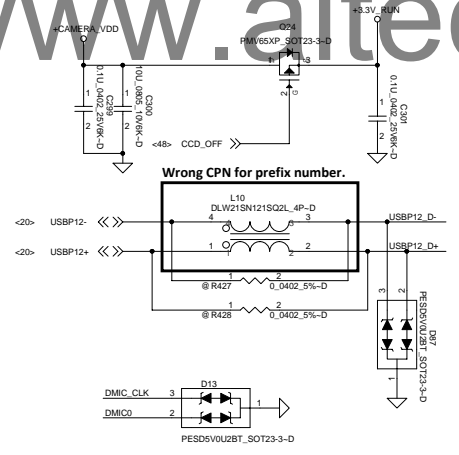
LCD Power



Panel backlight power control by EC



Webcam Circuit



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LVDS & CAM & TS

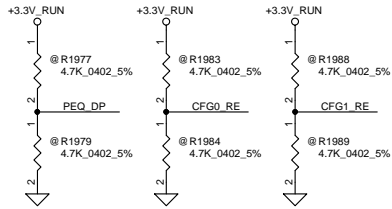
LA-7931P

Monday, July 23, 2012

Sheet 28 of 70

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DP v1.2 Redriver



Programmable input equalization levels; Internal pull down at -150k ohm, 3.3V I/O.

L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HBR2, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2

Configuration pin for automatic EQ and AUX interception; Internal pull down at -150k ohm, 3.3V I/O.

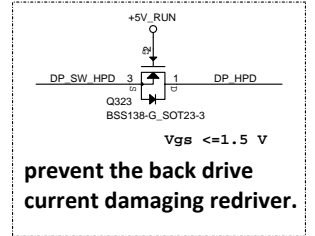
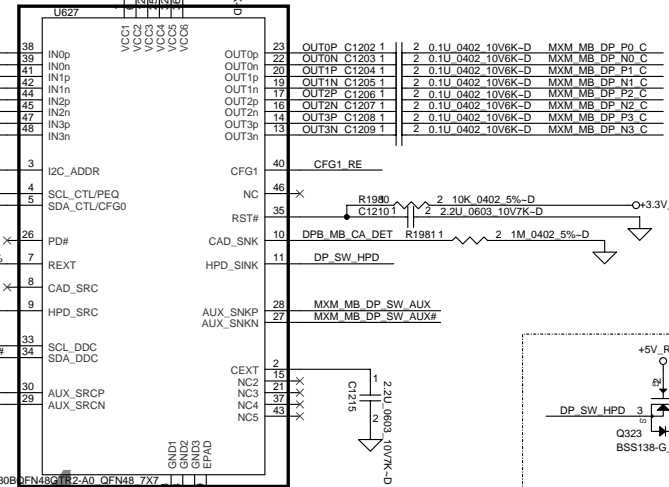
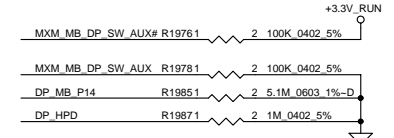
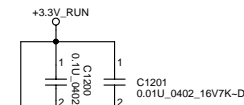
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing

Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at -150k

H: default, auto test disable & input offset cancellation enable
L: auto test enable & input offset cancellation enable
M: auto test disable & input offset cancellation disable

PD# : Internal pull up 150k ohm.

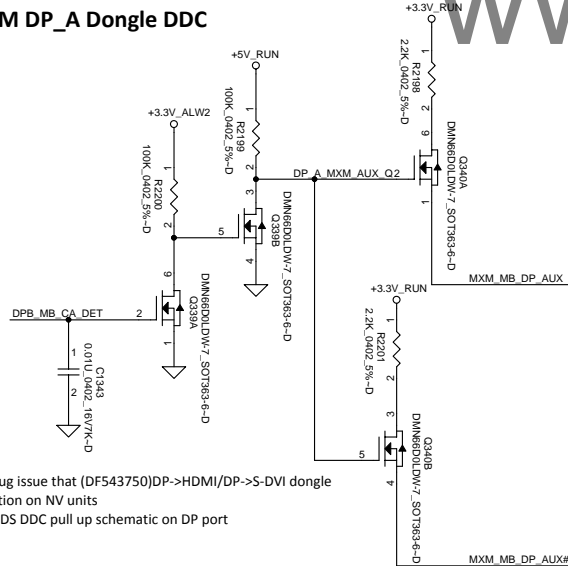
<16> MXM_MB_DP_AUX <<< MXM_MB_DP_AUX# C1213 1 2 0.1U 0402 10V6K-D AUX SRCP
<16> MXM_MB_DP_AUX# C1214 1 2 0.1U 0402 10V6K-D AUX SRCN



prevent the back drive current damaging redriver.

Solve DP->HDMI/DP->S-DVI dongle no function on NV units.

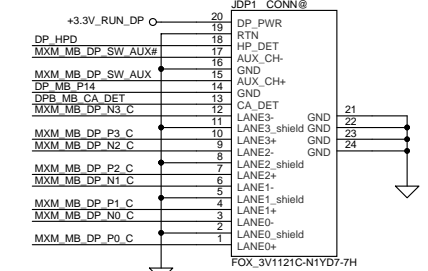
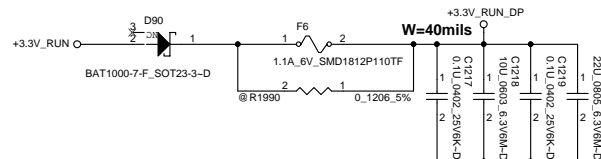
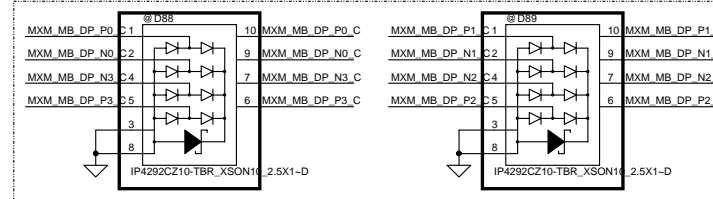
MXM DP_A Dongle DDC



For debug issue that (DF543750)DP->HDMI/DP->S-DVI dongle no function on NV units
Add TMDS DDC pull up schematic on DP port

According to new EIA rule and change package to GTFK2

Place close JDP ESD request change main source to SC300002F0L.

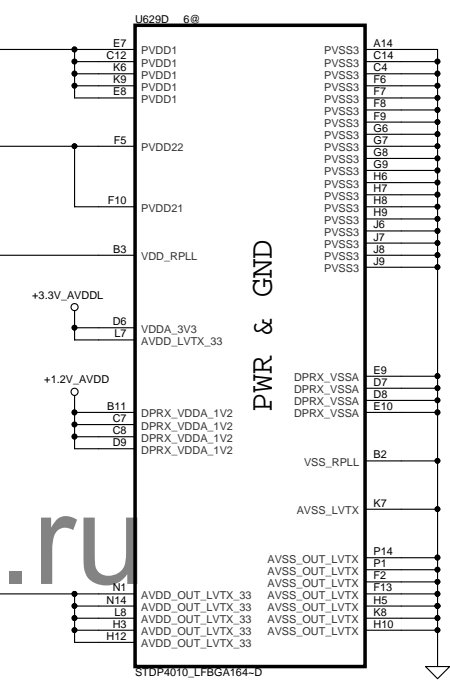
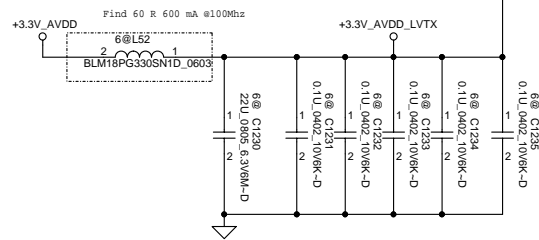
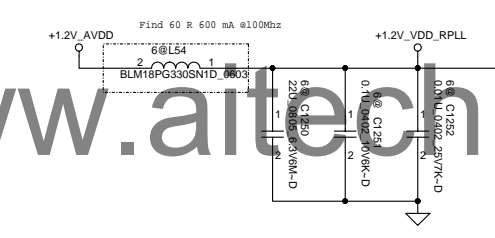
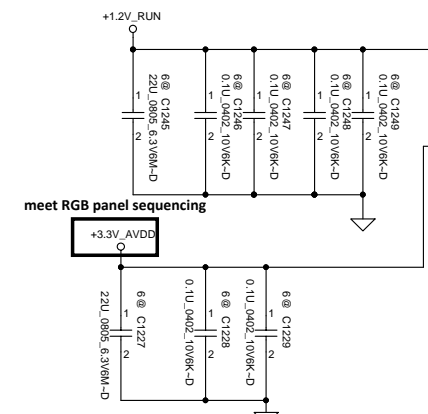
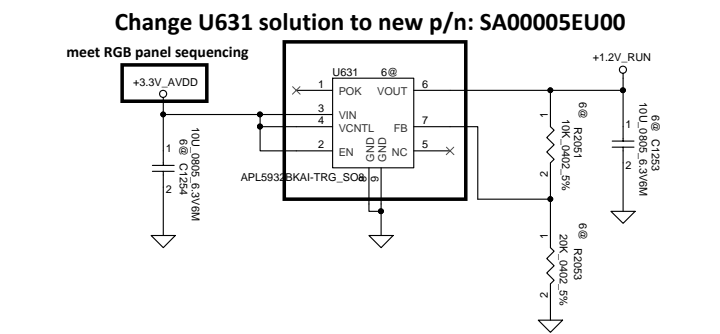
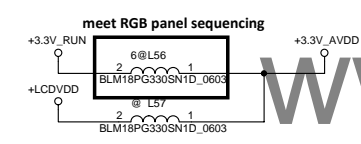
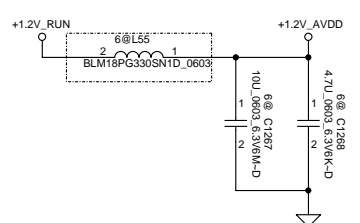
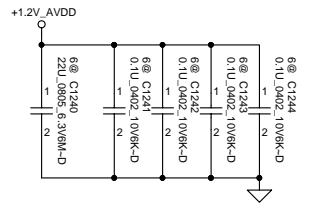
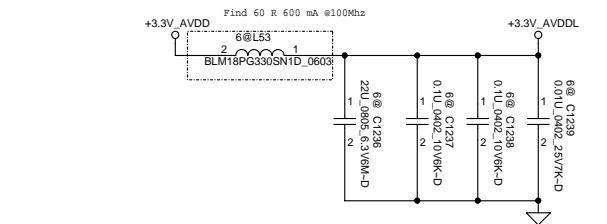


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DP Redriver & DP CONN			
Size	Document Number	Rev	
	LA-7931P	1.0	
Date:	Monday, July 23, 2012	Sheet	29 of 70

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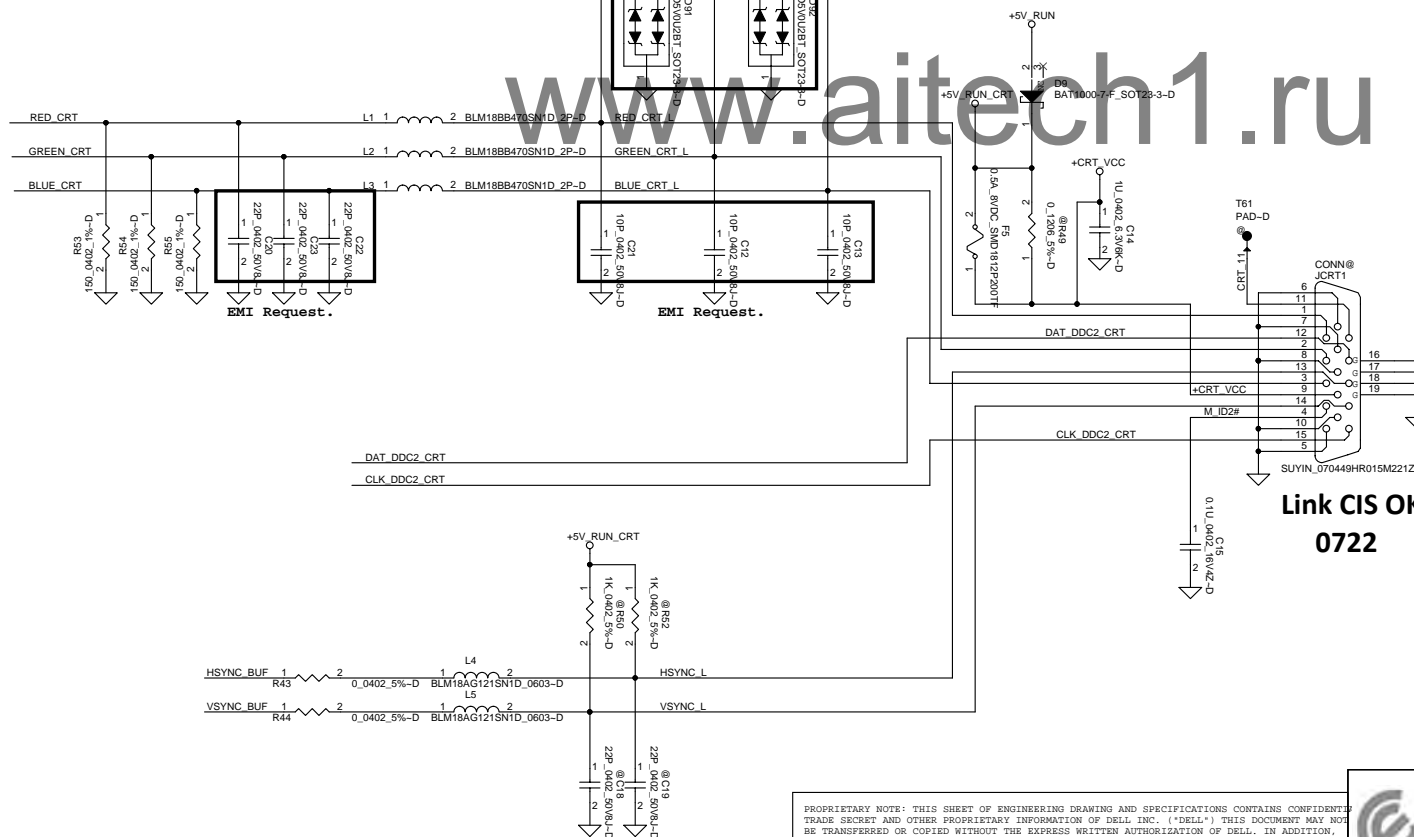
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eDP to LVDS(2)			
LA-7931P	Rev 1.0		
Monday, July 23, 2012	Sheet 31	of	70

Channel B --> PCH



CRT_SWITCH	0	0	1	1
DGPU_SELECT#	0	1	0	1
EDID_SELECT#	0	1	0	1
	A -> Port 1	B -> Port 1	A -> Port 2	B -> Port 2



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0722

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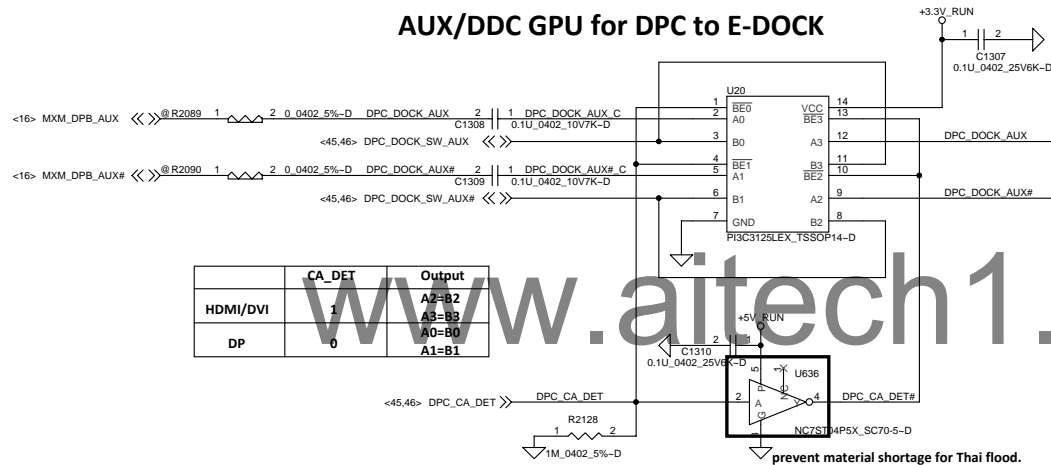
VGA

Size	Document Number	Rev
	LA-7931P	1.0

Date: Monday, July 23, 2012 Sheet 32 of 70

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AUX/DDC GPU for DPC to E-DOCK



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Compal Electronics, Inc.

Docking DP/DMC MUX

File
Size
Date: Monday, July 23, 2012

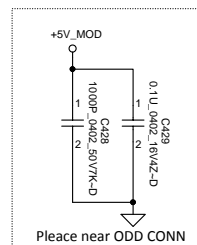
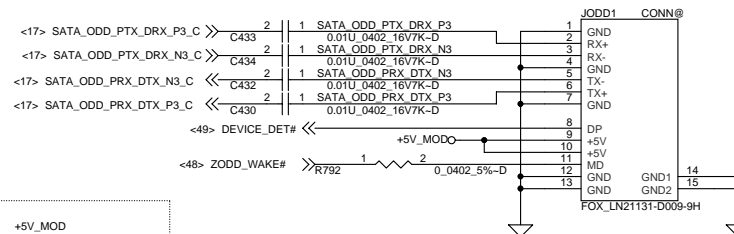
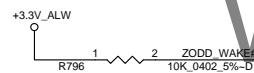
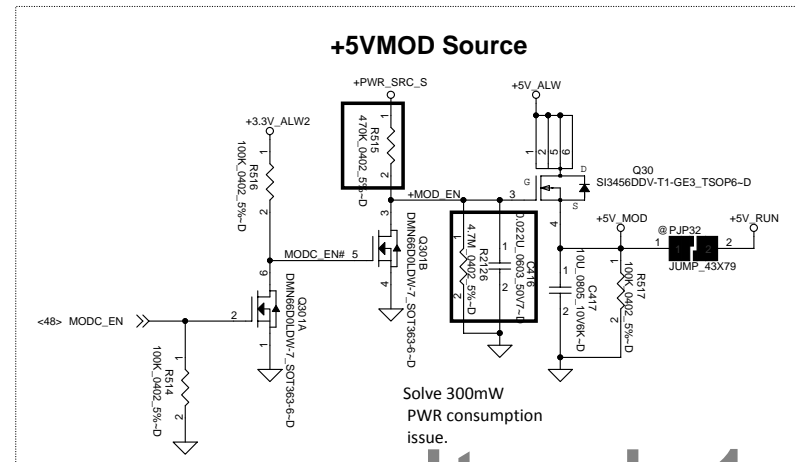
Document Number
LA-7931P

Rev
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Sheet 33 of 70

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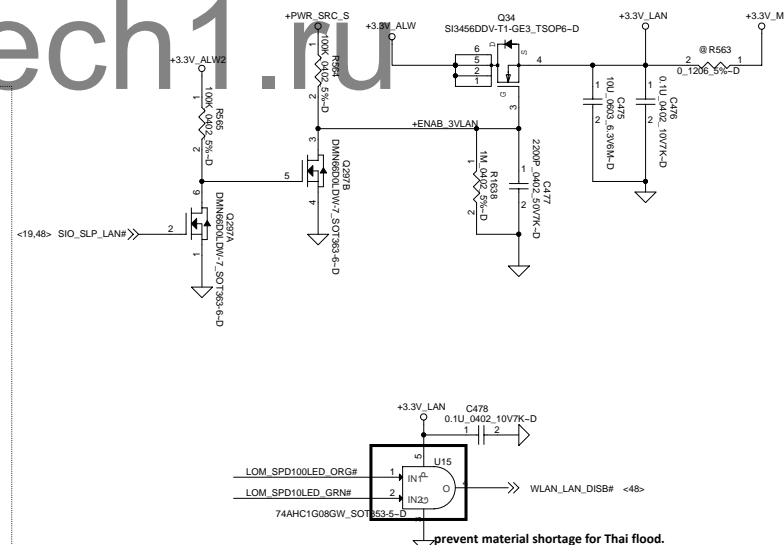
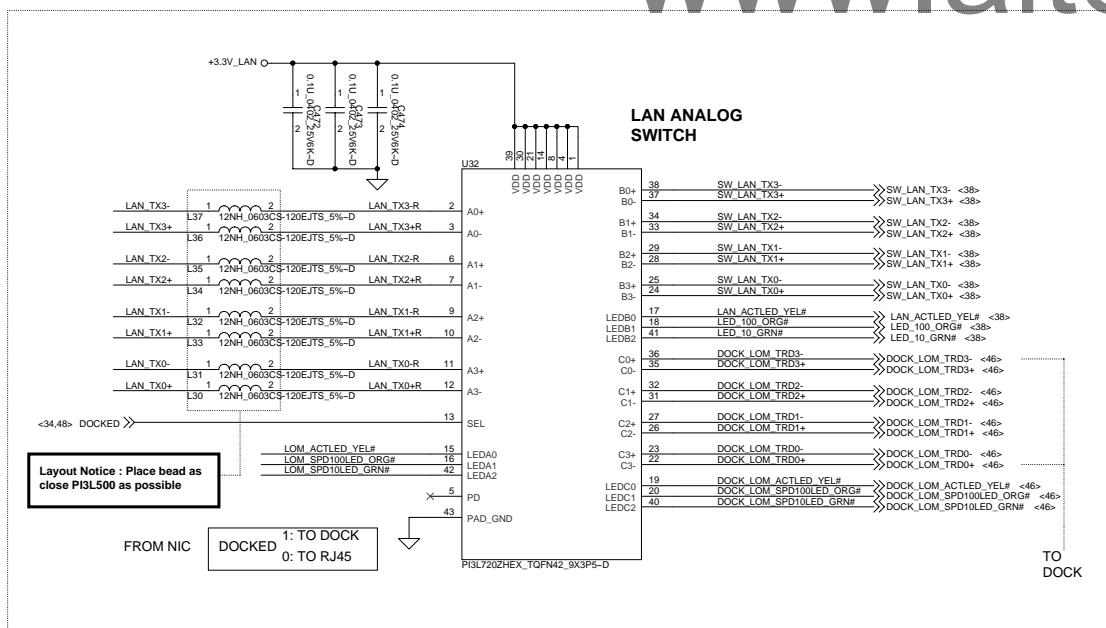
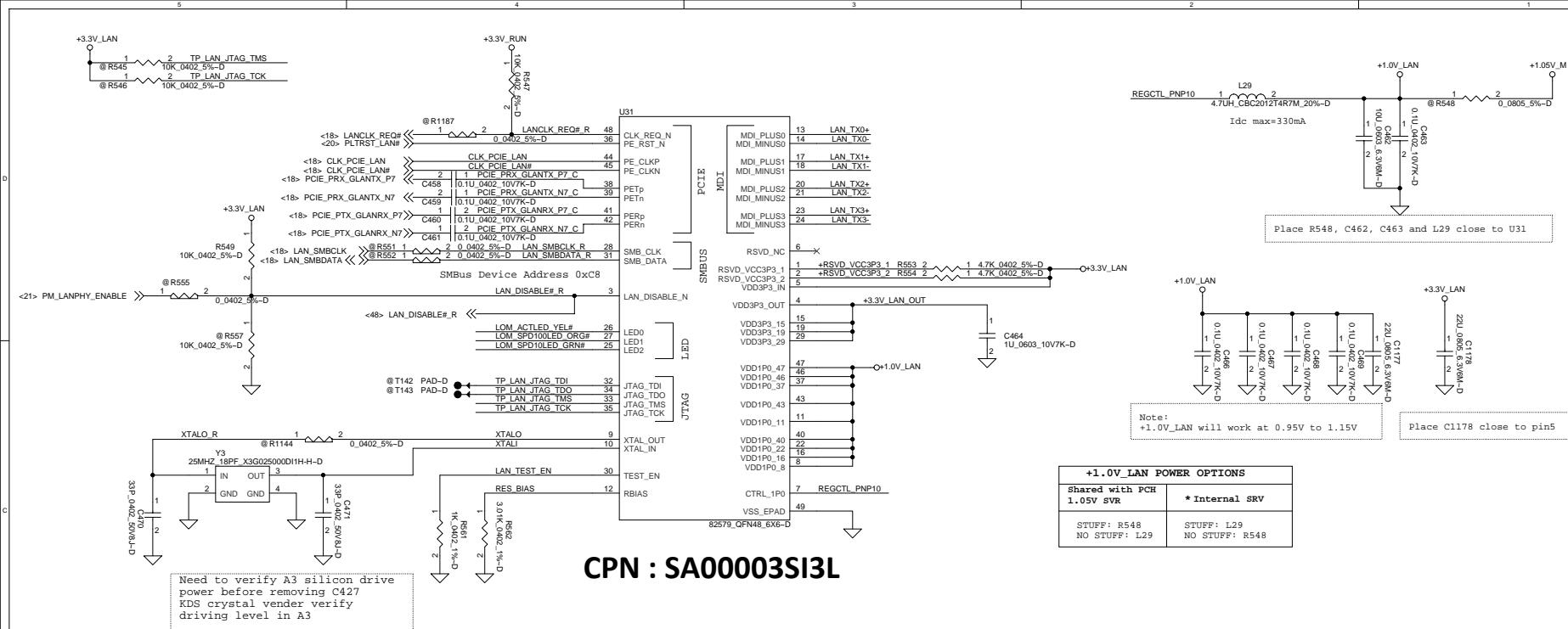
ODD CONN

LA-7931P

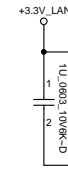
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Sheet 36 of 70

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T156			
1	TD1+	TX1+	24 NB_LAN_TX0+
2	TD1-	TX1-	23 NB_LAN_TX0-
3	TDCT1	TXCT1	22 Z2805
4	TDCT2	TXCT2	21 Z2807
5	TD2+	TX2+	20 NB_LAN_TX1+
6	TD2-	TX2-	19 NB_LAN_TX1-
7	TD3+	TX3+	18 NB_LAN_TX2+
8	TD3-	TX3-	17 NB_LAN_TX2-
9	TDCT3	TXCT3	16 Z2806
10	TDCT4	TXCT4	15 Z2808
11	TD4+	TX4+	14 NB_LAN_TX3+
12	TD4-	TX4-	13 NB_LAN_TX3-



The diagram shows the ICOM1 connector with the following connections:

- Signal Traces:**
 - <37> LAN_ACTLED_YEL#**: Connected to pin 13 (R1171, 150_0402_5%-D).
 - <37> LED_10_GRN#**: Connected to pin 10 (R1170, 150_0402_5%-D).
 - <37> LED_100_ORG#**: Connected to pin 11 (R1167, 150_0402_5%-D).
- LED Connections:**
 - Yellow LED-**: Connected to pin 12.
 - Yellow LED+**: Connected to pin 13.
 - Green LED-**: Connected to pin 9.
 - LED+**: Connected to pin 10.
 - ORANGE LED-**: Connected to pin 11.
- Other Connections:**
 - +3.3V_LAN**: Connected to pin 13.
 - SHLD2**: Connected to pin 15.
 - SHLD1**: Connected to pin 14.

A note indicates: **for ESD Hi-Pot fail.** with a diagram showing a connection from pin 14 to a ground symbol.

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0722

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RJ45

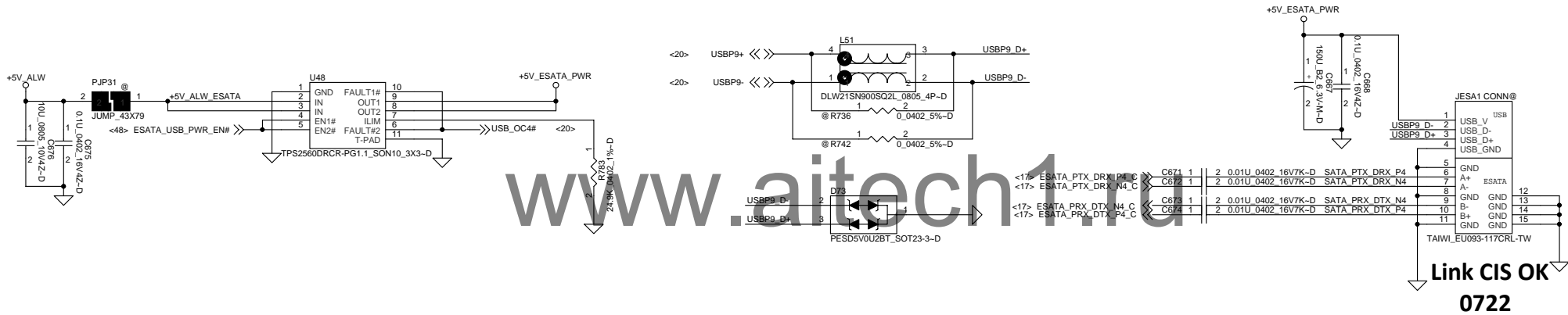
LA-7931P

Rev	1.0
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Date: Monday, July 23, 2012

Sheet 38 of 70

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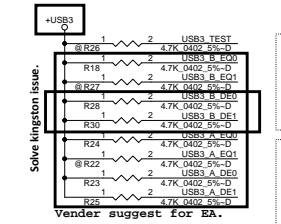
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Title ESATA		
Size	Document Number LA-7931P	Rev 1.0
Date	Monday, July 23, 2012	Sheet 39 of 70

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For USB3 redriver 2nd source

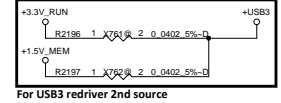


EQ : Equalizer control and program, 3.3V tolerant. Internally pulled down at ~150K ohm
[A, EQ1, A, EQ0] ==
L: program EQ for channel loss up to 4.5dB
LH: program EQ for channel loss up to 7.5dB
HL: program EQ for channel loss up to 9.5dB
HLL: program EQ for channel loss up to 13dB

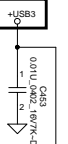
TEST : Chip test mode enable, 3.3V tolerant. Internally pulled down at ~150K ohm.
L: Normal operation (default)
H: Test mode enable
for compliance test, this pin should be pulled to high.

DE : Programmable output pre-emphasis level setting, 3.3V tolerant. Internally pulled down at ~150K ohm
[A, DE1, A, DE0] ==
L: 3.5dB de-emphasis
LL: 5.5dB de-emphasis
HL: 2.7dB de-emphasis
HH: 5dB de-emphasis

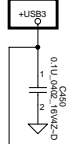
Pin 13 : B, EQ0 / SDA_CTL Pin28 : A, DE1 / NC
Pin 14 : B, EQ1 / SCL_CTL Pin29 : A, DE0 / NC
Pin 15 : B, DE0 / I2C_ADDR0 Pin31 : A, EQ1 / NC
Pin 16 : B, DE1 / I2C_ADDR1 Pin32 : A, EQ0 / NC



For USB3 redriver 2nd source

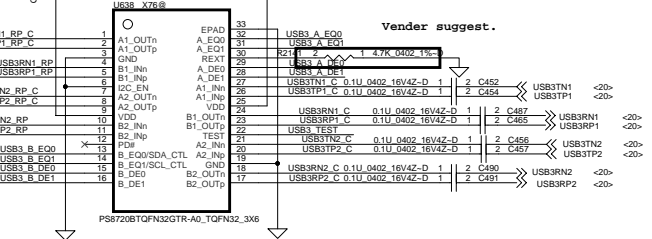


For USB3 redriver 2nd source



HDD Redriver Select Component			
	X76(Main)	X76(2nd)	
	X7641231L03	X7641231L04	
	PS8720B	PS8720A	
	SA00004UI00	SA00005PO00	
U638	V	V	
R2196	V		
R2197		V	

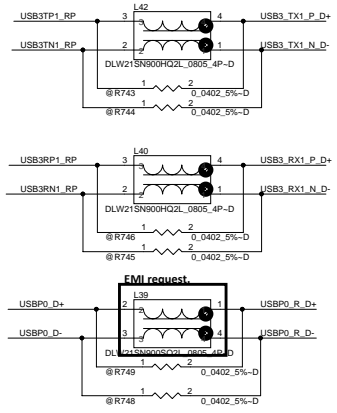
Vendor suggest.



PD1: chip power down, active LOW, 3.3V tolerant, internally pulled up at ~150K ohm.

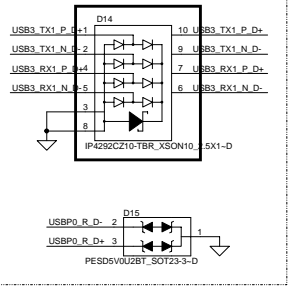


For EMI request

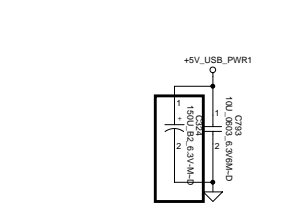
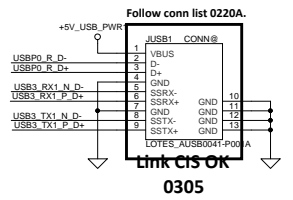


BSD request change main source to SC300002F0L.

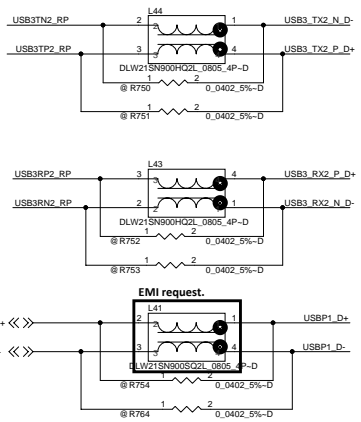
For ESD request



NEC_TOKIN shortage issue for the flood in Tailand and small size for ME space.

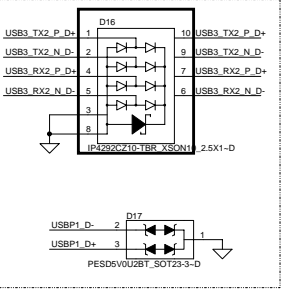


For EMI request

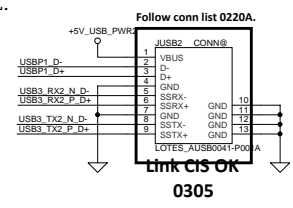


BSD request change main source to SC300002F0L.

For ESD request



NEC_TOKIN shortage issue for the flood in Tailand.



CB=0	autodetection charger identification active
CB=1	charging downstream port with active USB2.0 data communication mode with 1.5A support

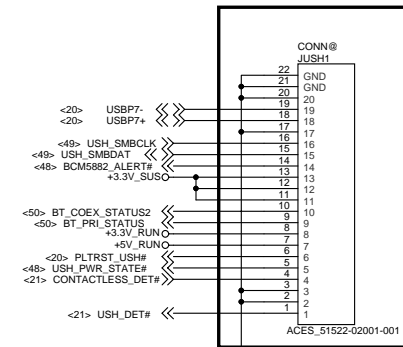
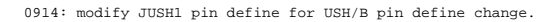
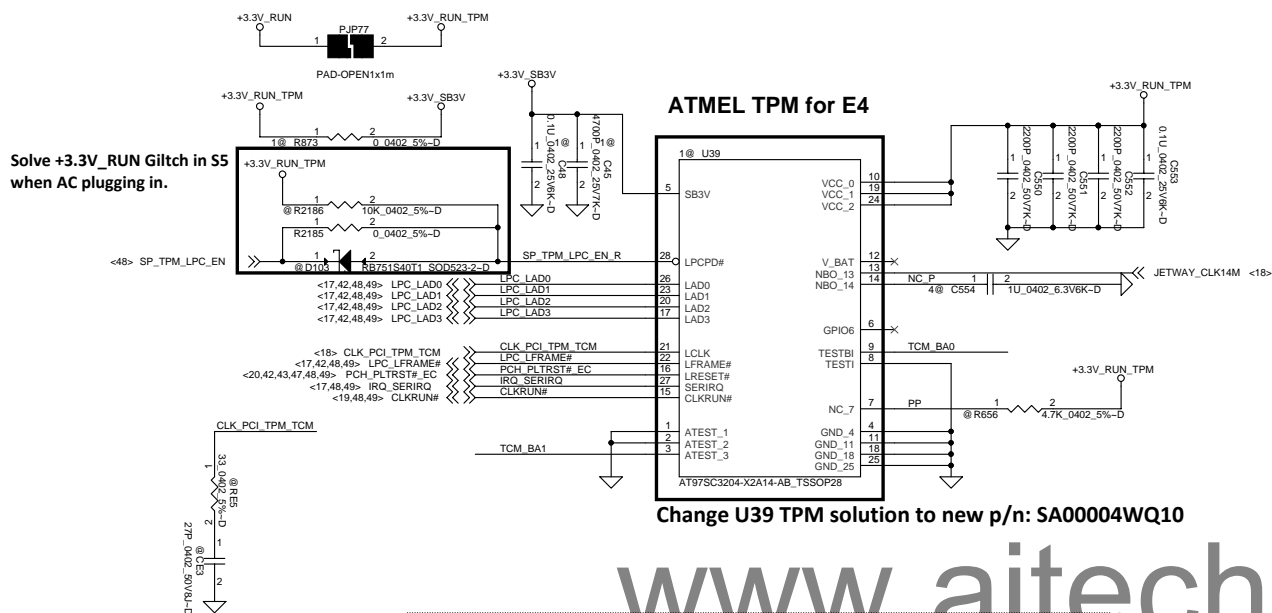
CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

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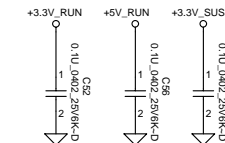
Compal Electronics, Inc.

Title	USB3.0
Size	Document Number
Rev	LA-7931P
Date	Monday, July 23, 2012
Sheet	40 of 70

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0722

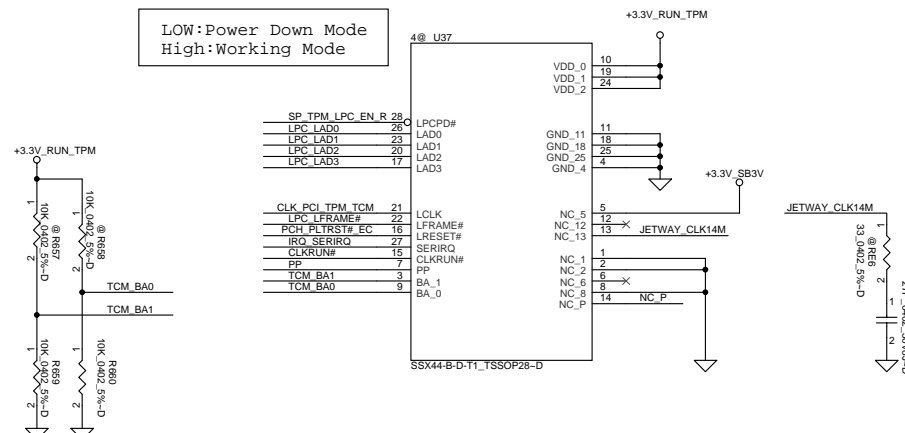


Change U39 TPM solution to new p/n: SA00004WQ10

Co-lay U37 and U39

LPC layout: Place TCM first and then end LPC with TPM.

China TCM: NationZ & Jetway co-lay



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TPM/TCM

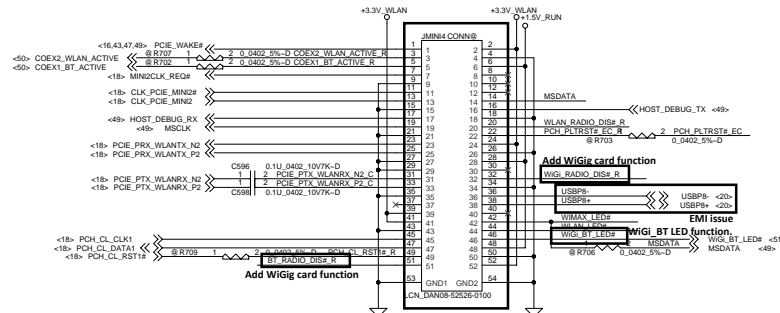
LA-7931P

Rev	1.0
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Date: Monday, July 23, 2012

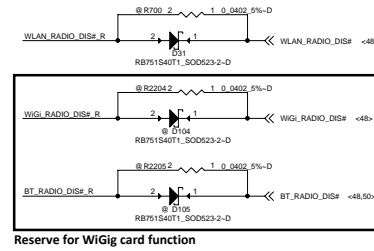
Sheet 41 of 70

Mini WLAN/WIMAX/WiGig H=4

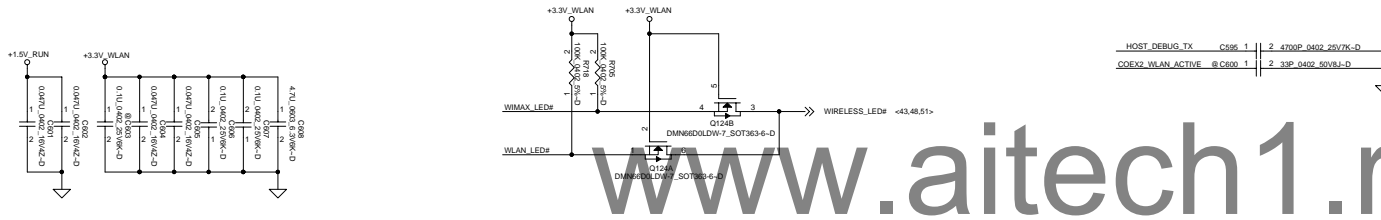


follow connector list 1005: AAA-PCI-092-P01_A footprint same as DAN08-52526-0100. next phase need change.

Link CIS OK_0722

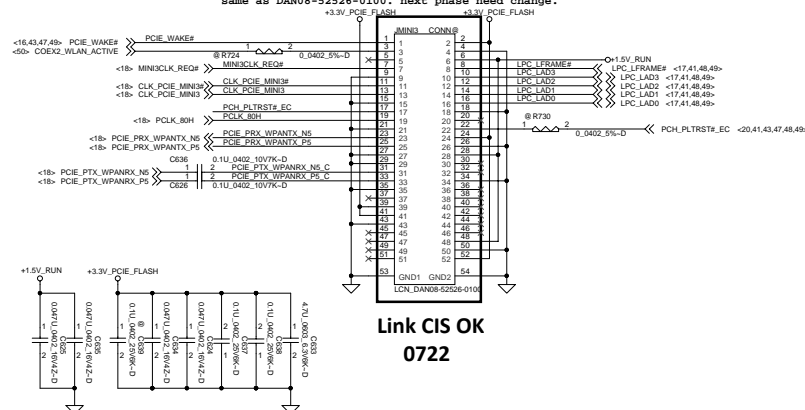


Reserve for WiGig card function



1/2 Minicard Pink Pather

follow connector list 1005: AAA-PCI-092-P01_A footprint same as DAN08-52526-0100. next phase need change.



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0722

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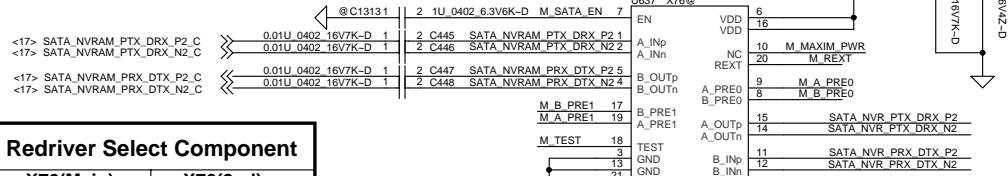
Mini Card-1/2

LA-7931P

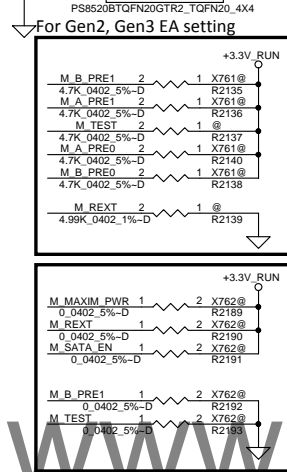
Date: Monday, July 23, 2012 Sheet 42 of 70

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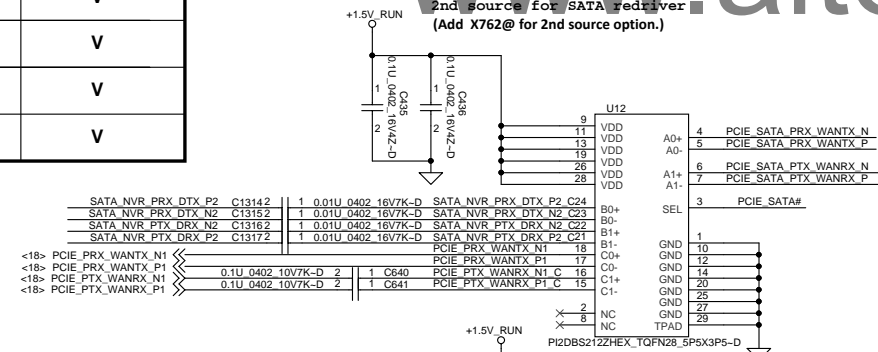
SATA Repeater



HDD Redriver Select Component		
	X76(Main) X7641231L01	X76(2nd) X7641231L02
	PARADE(Main) SA00004WF00	MAXIM(2nd) SA00002EY1L
U637	V	V
R2135	V	
R2136	V	
R2137		
R2140	V	
R2138	V	
R2139		
R2189		V
R2190		V
R2191		V
R2192		V
R2193		V

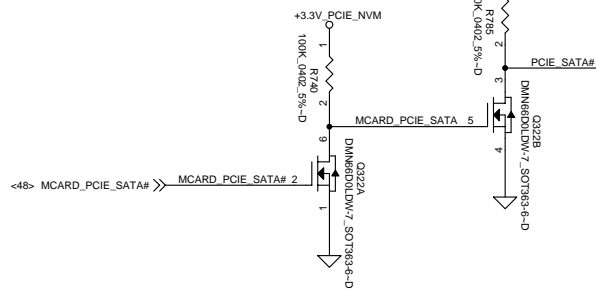


2nd source for SATA redrive
(Add X762@ for 2nd source option.)

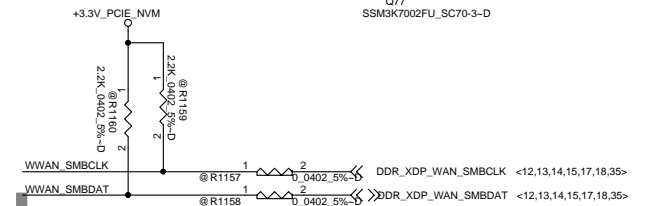
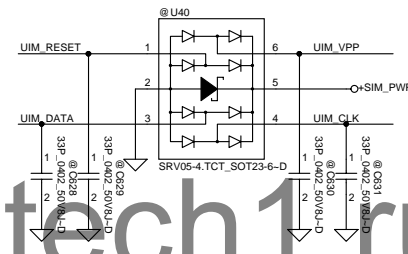
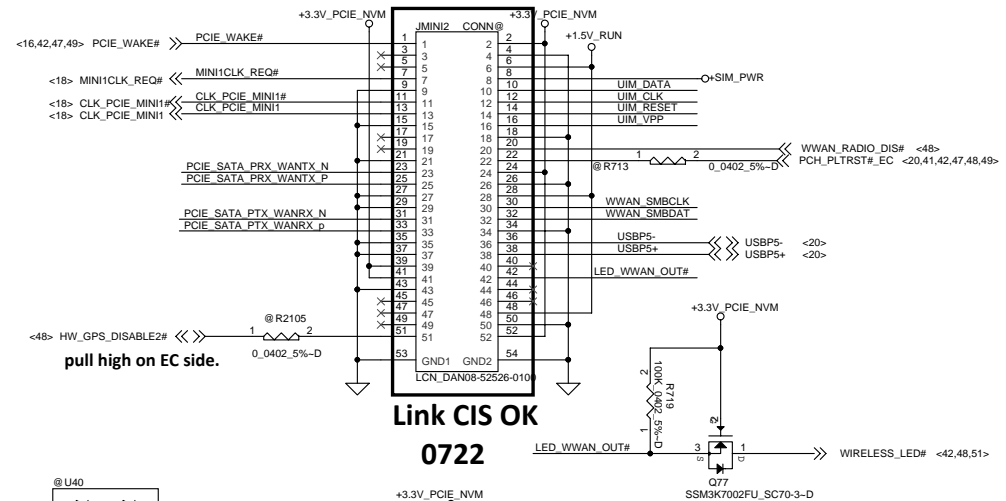


PIN	mSATA	WWAN
23	TX+	PERn0
25	TX-	PERp0
31	RX-	PETn0
33	RX+	PETp0

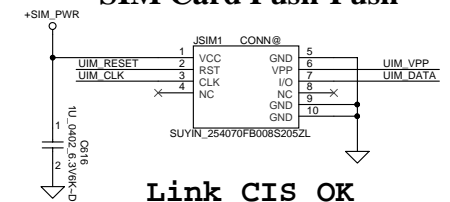
Function	SEL
Port A to Port B	L
Port A to Port C	H



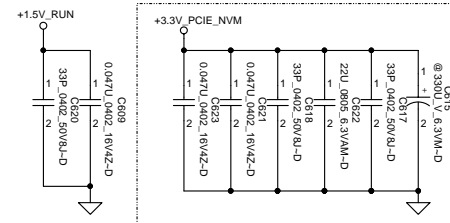
Mini WWAN/GPS/LTE/mSATA
follow connector list 1005: AAA-PCI-092-P01_A footprint
same as DAN08-52526-0100. next phase need change.



SIM Card Push-Push



Link CIS OK
0722



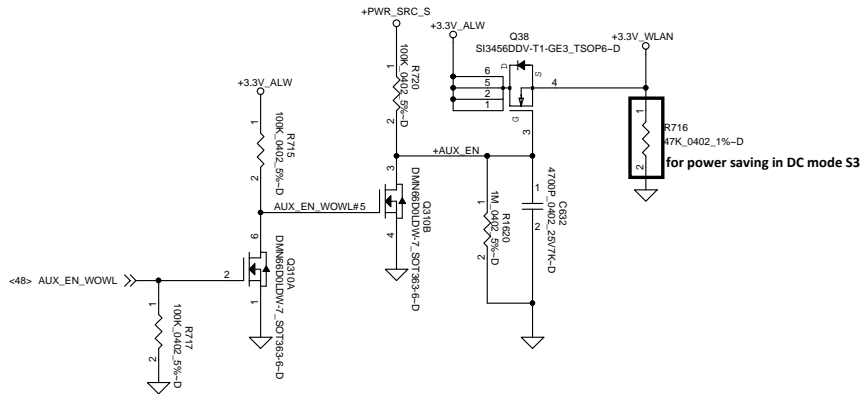
For RF layout request

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+9%	1000	750	
+3.3Vaux	+9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+5%	500	375	NA

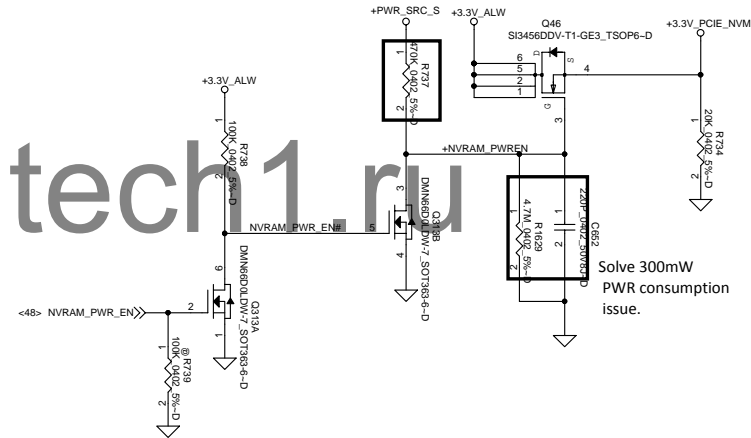
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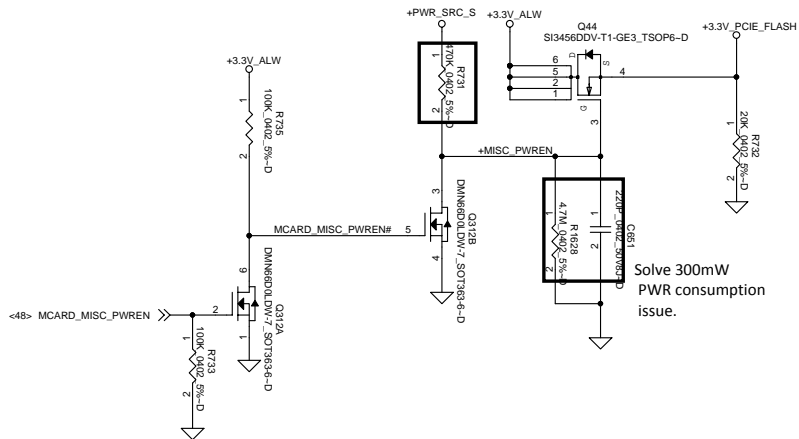
Power Control for Mini card1



Power Control for Mini card2



Power Control for Mini card3



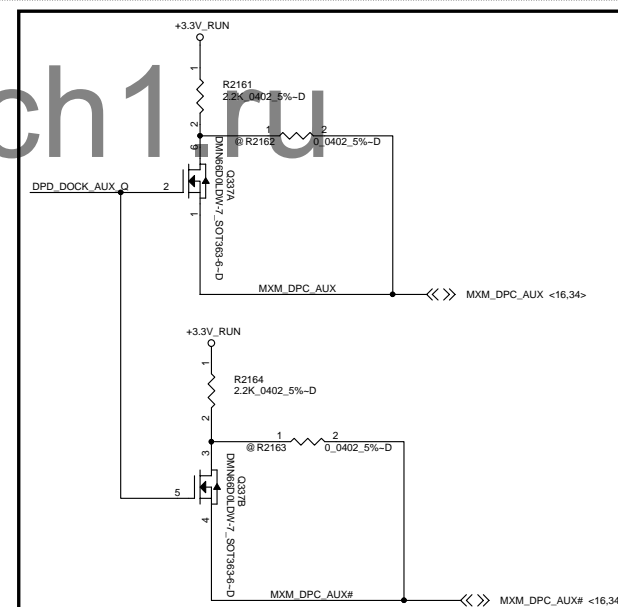
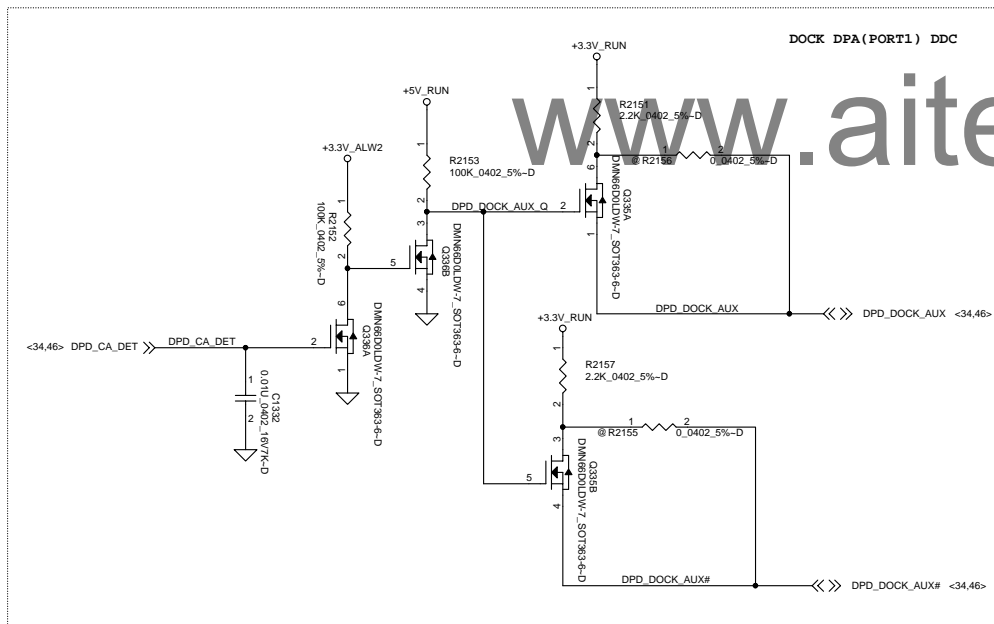
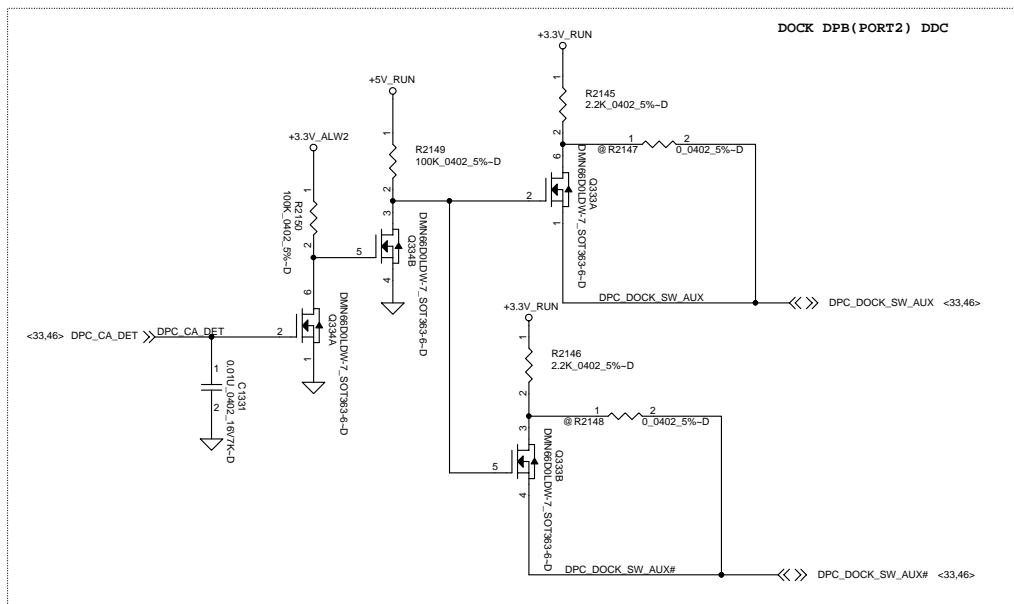
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Mini Card PWR

File	Document Number	Rev
LA-7931P	1.0	
Date	Monday, July 23, 2012	Sheet 44 of 70

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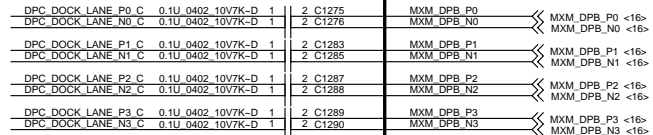
DOCK DP DDC SW

LA-7931P

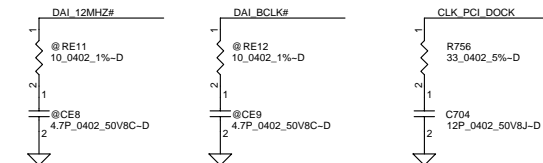
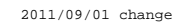
Rev	1.0
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Date: Monday, July 23, 2012

Sheet 45 of 70

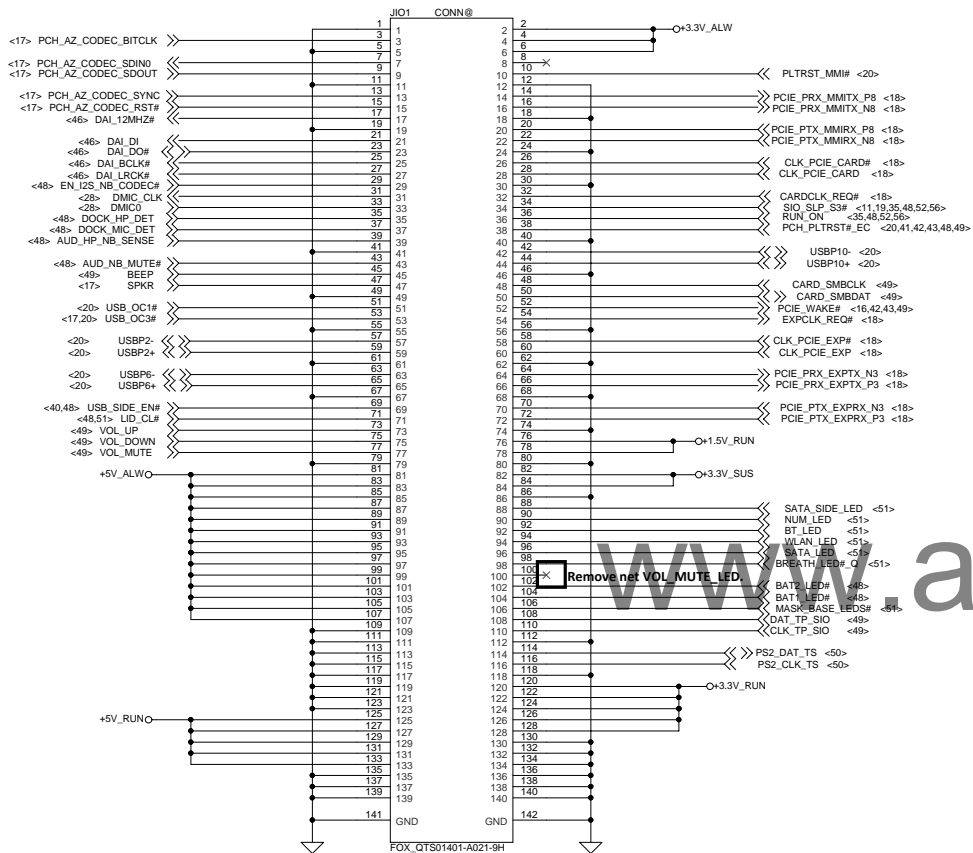


reduce layout via

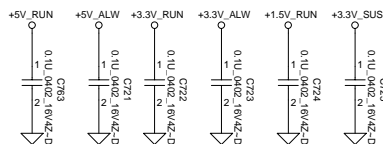


Title			
Docking			
Size	Document Number	LA-7931P	Rev 1.0
Date:	Monday, July 23, 2012	Sheet 46 of 70	

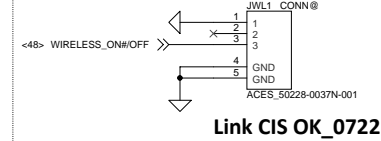
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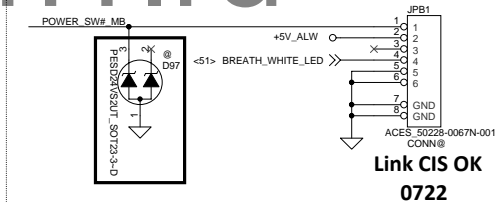
Link CIS OK
0722



Wireless ON/OFF CONN

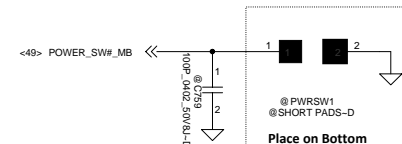


Power Bottom CONN



ESD request reserve it.

Power Switch for debug

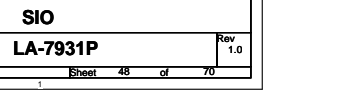
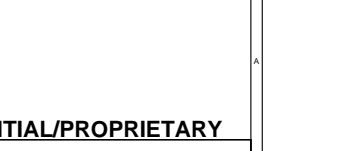
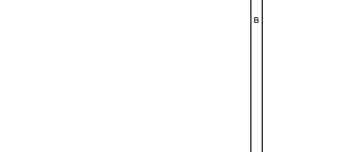
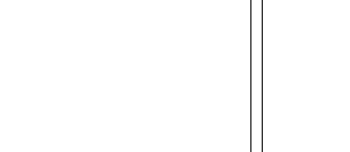
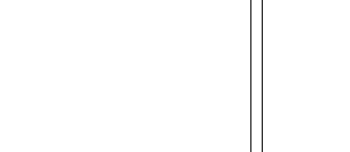
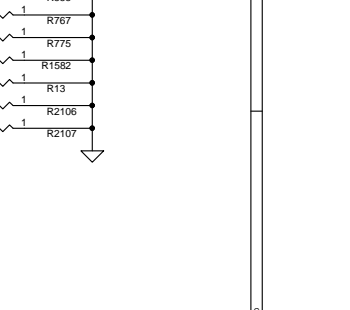
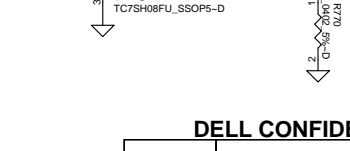
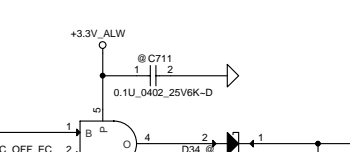
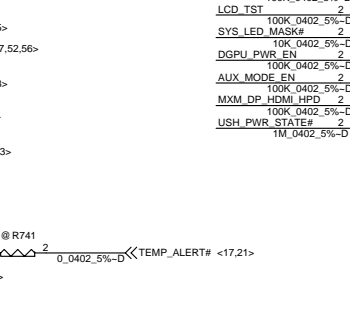
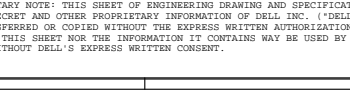
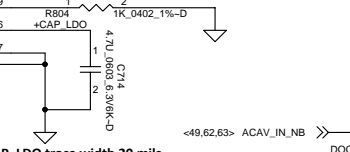
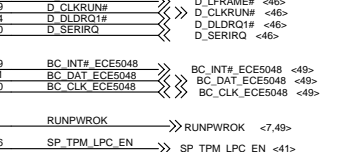
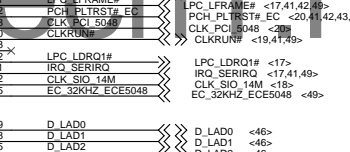
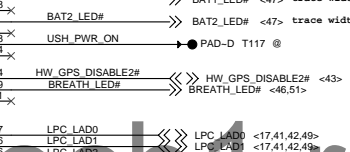
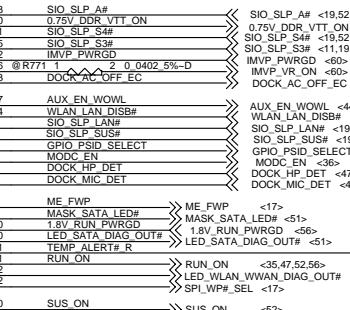
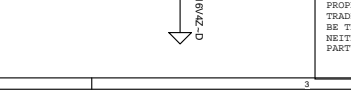
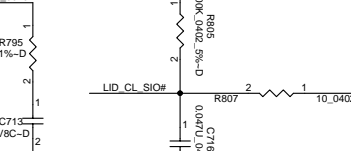
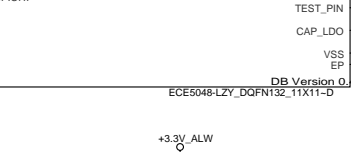
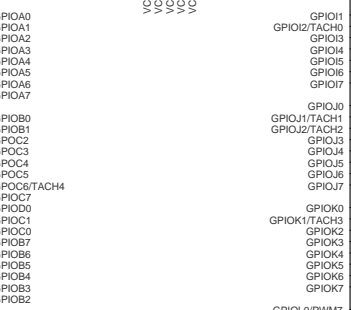
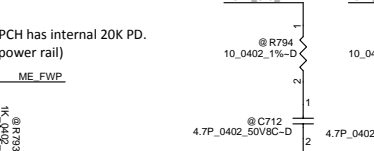
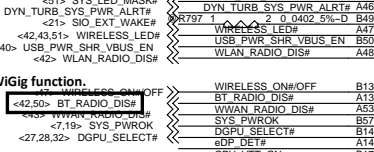
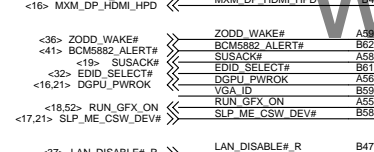
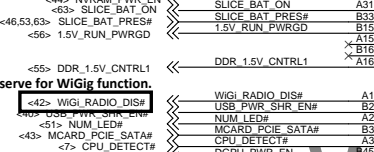
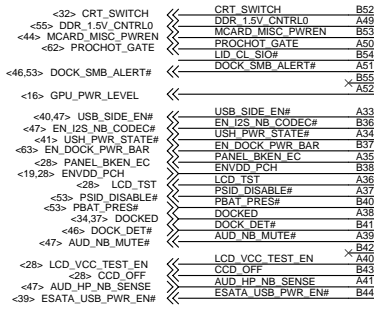
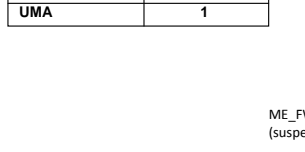
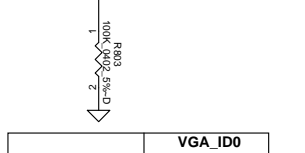
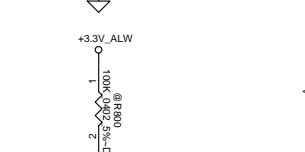
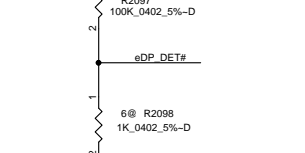
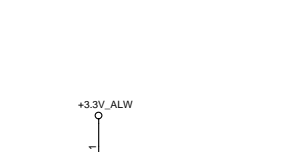
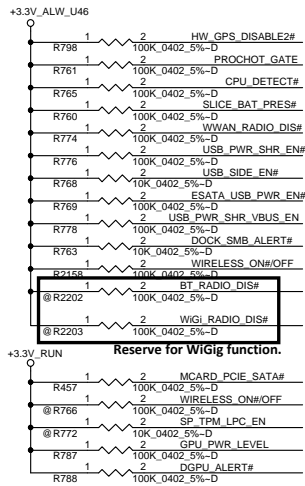


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Compal Electronics, Inc.

File	I/O board		
Size	Document Number	LA-7931P	Rev 1.0
Date:	Monday, July 23, 2012	Sheet 47	of 70

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ME_FWP PCH has internal 20K PD.
(suspend power rail)

+CAP_LDO trace width 20 mils

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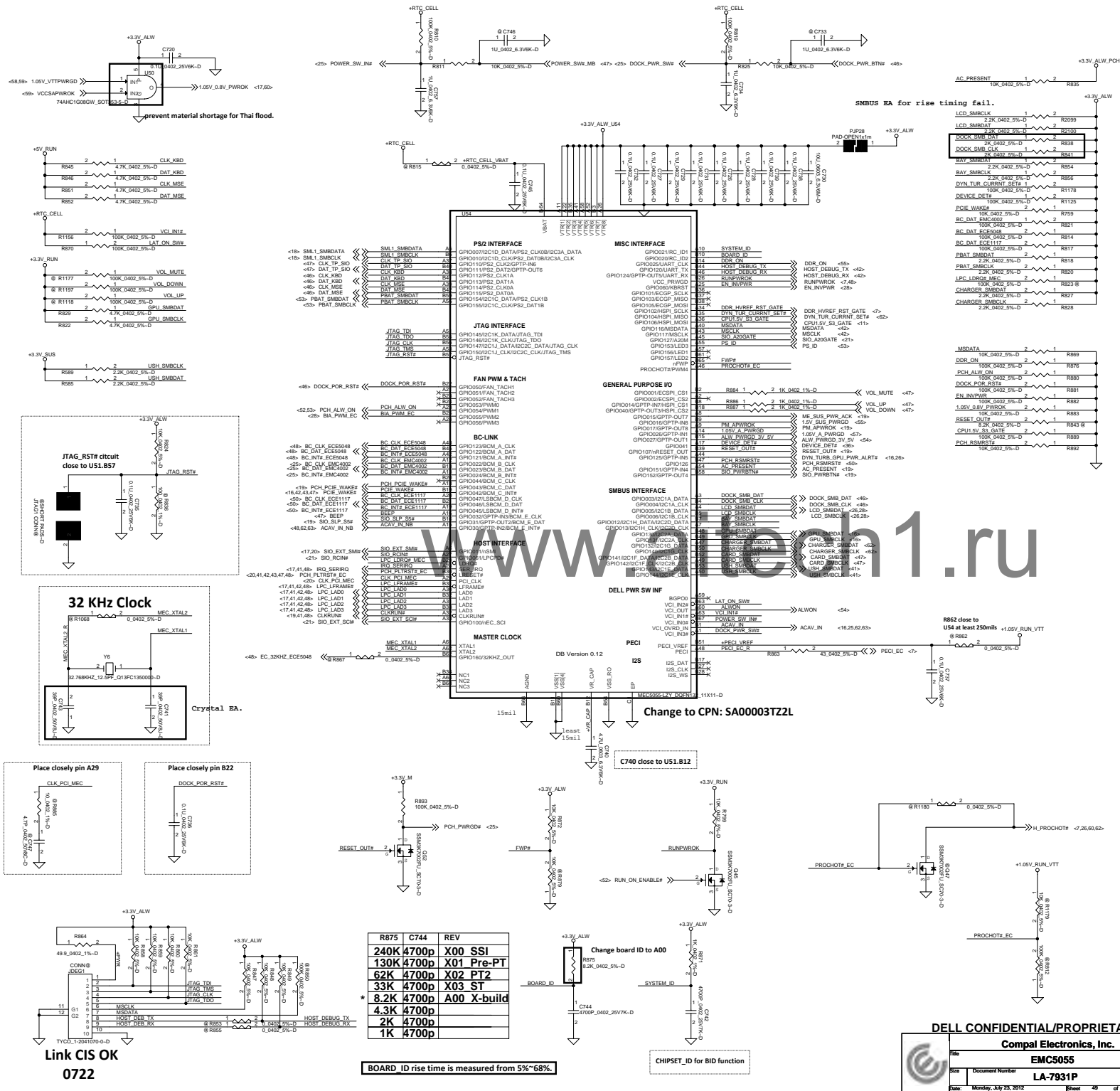
Compal Electronics, Inc.

SIO

LA-7931P

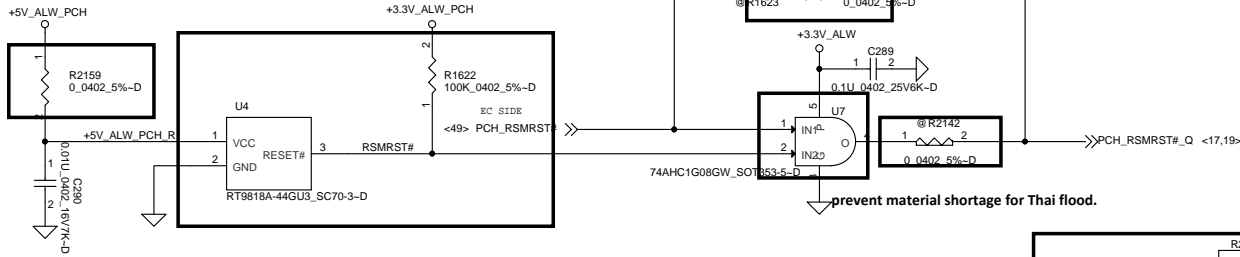
Date: Monday, July 23 2012 Sheet 48 of 70

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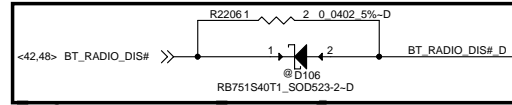


RSMRST circuit

For meet T235(power off)= min 40ns(SPEC).T08a(power on)= max 90ms.



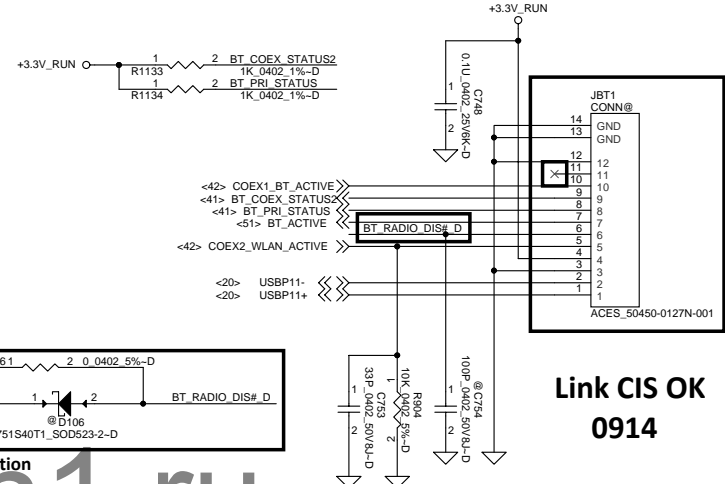
prevent material shortage for Thai flood.



Reserve for WiGig card function

BlueTooth

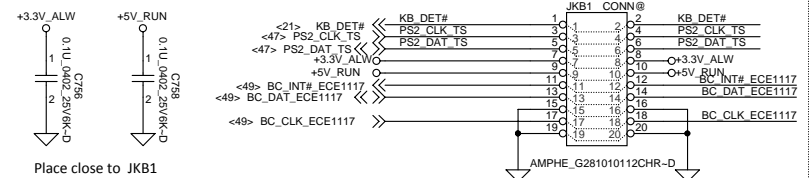
JBT1 pin11 Need confirm with Dell to add BT_DET or not.



Link CIS OK
0914

JBT1 pin1-pin12 pin define order swap to pin12-pin1 for BT connector change to ACES_50450-0127N-001.
(because footprint different from ACES_50228-0127N_001)

Keyboard



Place close to JKB1

Link CIS OK
0722

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Touch PAD/Int KB

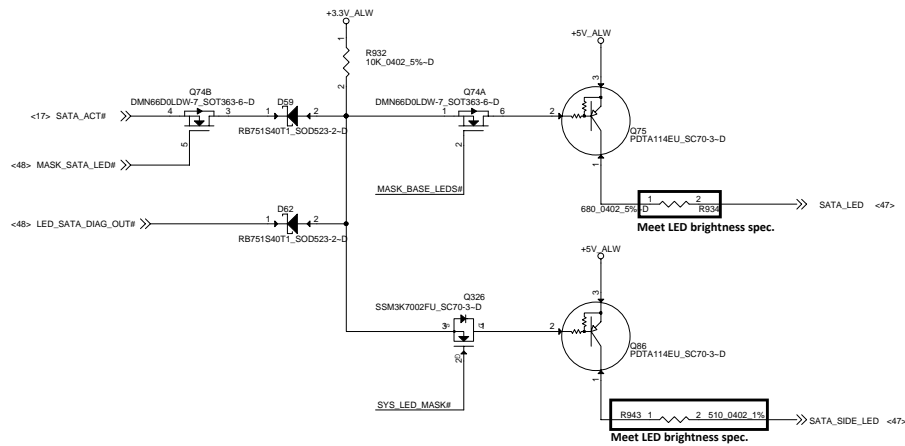
LA-7931P

Rev 1.0

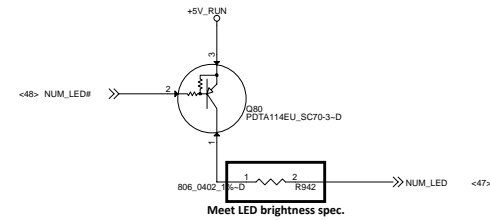
Date: Monday, July 23, 2012 Sheet 50 of 70

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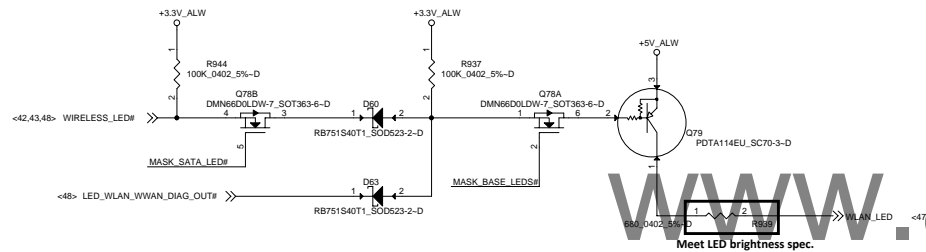
HDD LED



NUM LED

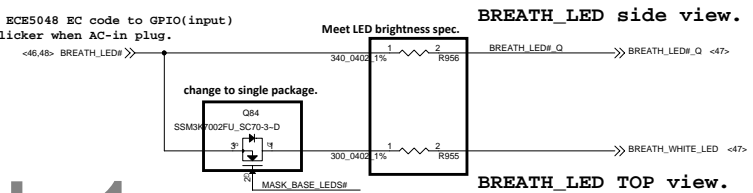


WWAN/WLAN LED



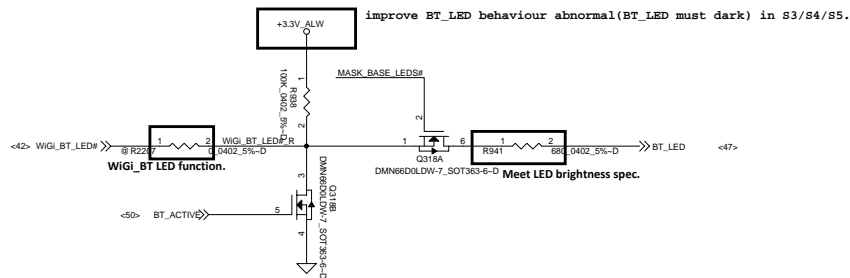
Breath LED

Change B39 of ECE5048 EC code to GPIO(input)
Solving LED flicker when AC-in plug.

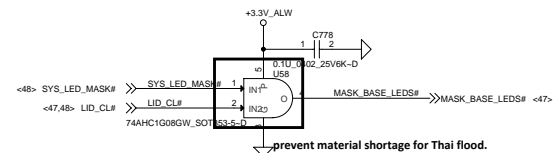


BT LED

improve BT_LED behaviour abnormal(BT_LED must dark) in S3/S4/S5.



Remove Q339 for WiGig card function usage.

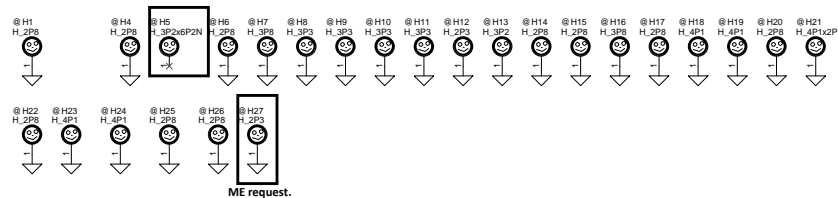


LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark

- @FD1
FIDUCIAL MARK-D
- @FD2
FIDUCIAL MARK-D
- @FD3
FIDUCIAL MARK-D
- @FD4
FIDUCIAL MARK-D

for Hi-POT issue.



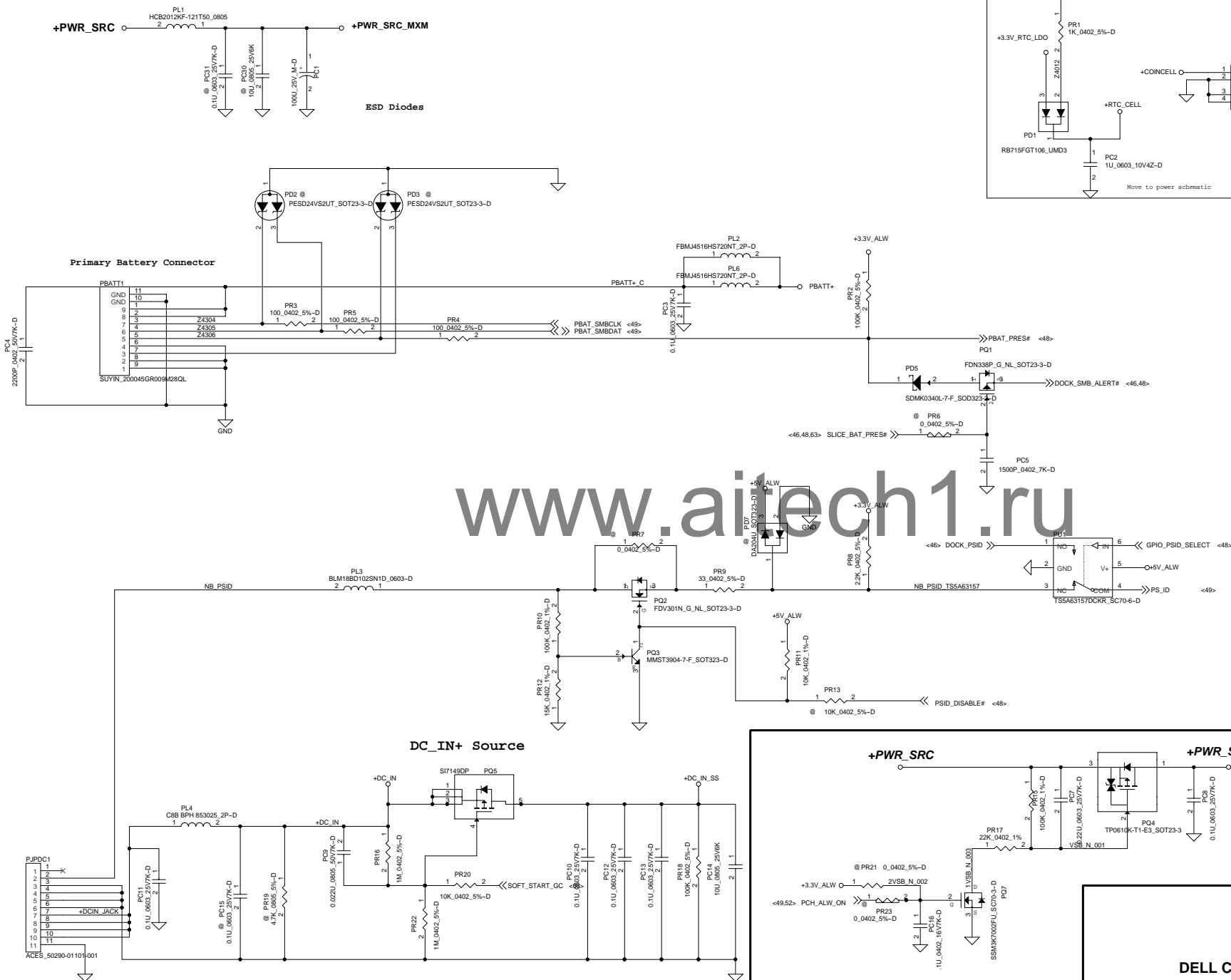
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PAD & Standoff & LED

File	Document Number	Rev
Size	LA-7931P	1.0
Date	Monday, July 23, 2012	Sheet 51 of 70



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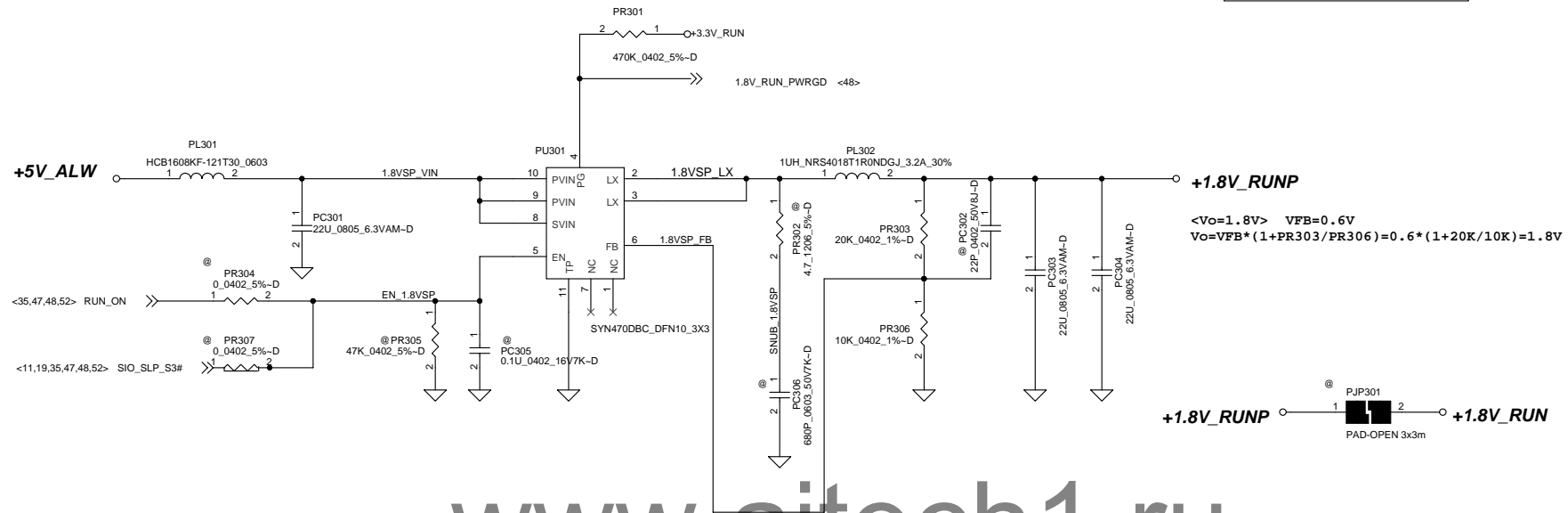
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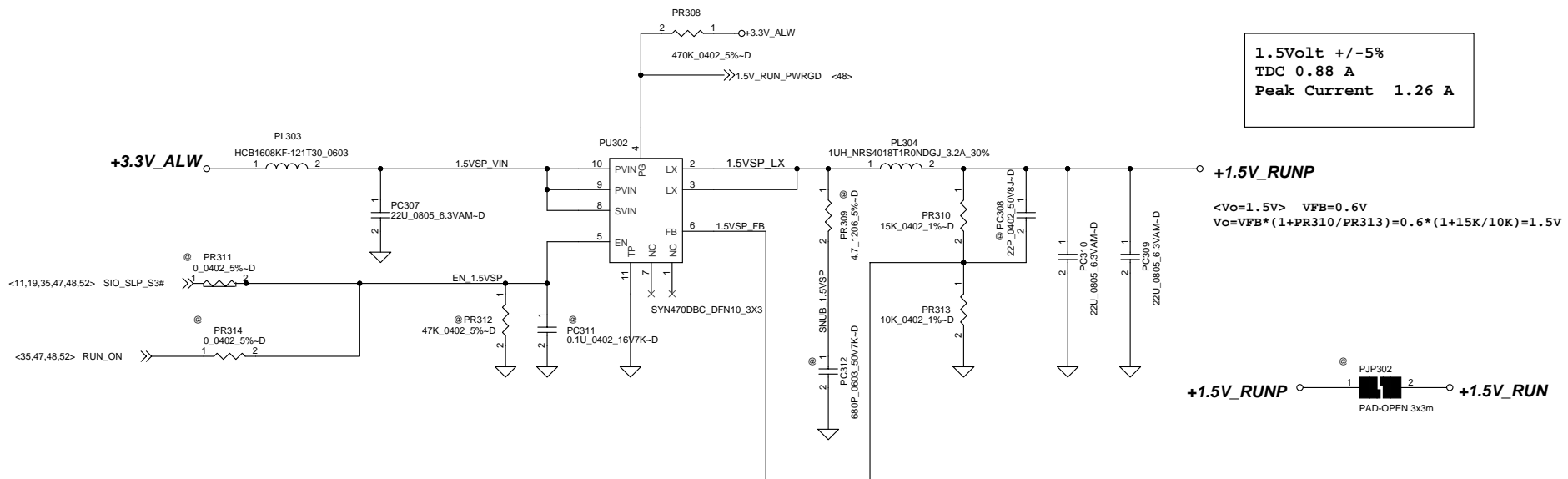
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Size: Document Number
Date: Monday, July 23, 2012
Sheet 53 of 70

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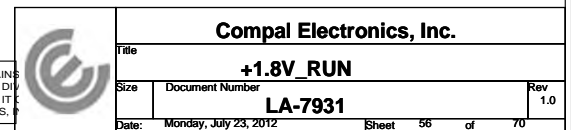

```
1.8Volt +/-5%
TDC 0.65A
Peak Current 0.93A
```



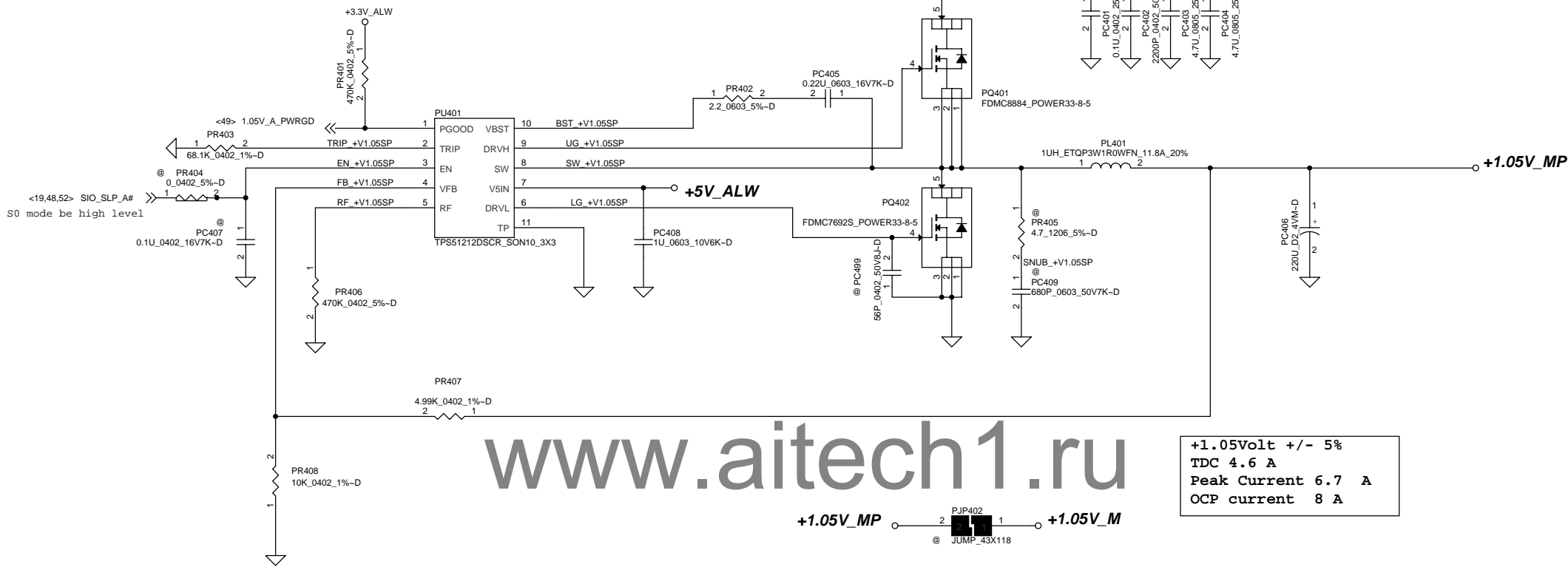
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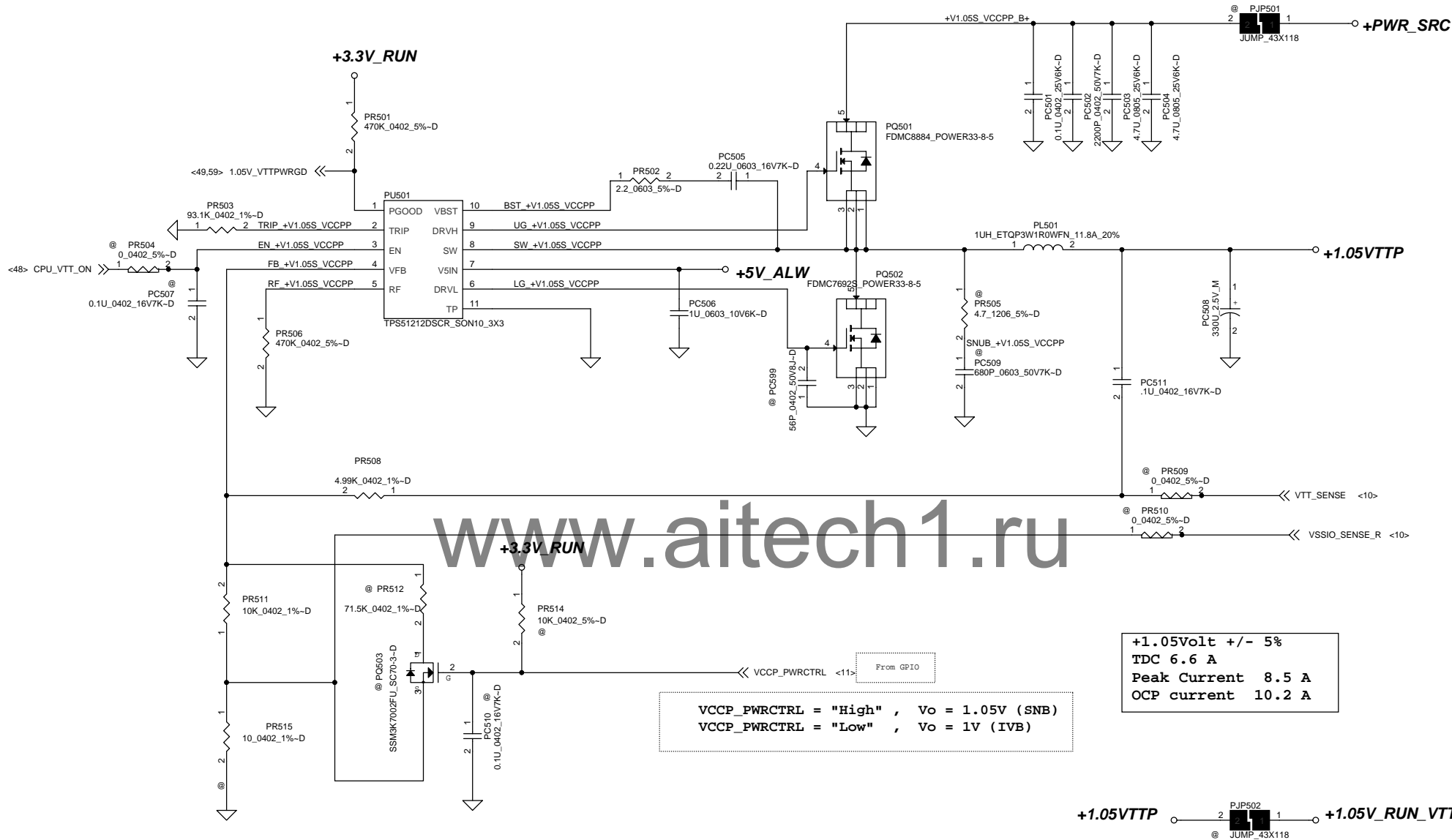
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Title		+1.05V_M	
Size	Document Number	Rev	
	LA-7931	1.0	
Date:	Monday, July 23, 2012	Sheet	57 of 70



+1.05Volt +/- 5%
TDC 6.6 A
Peak Current 8.5 A
OCP current 10.2 A

VCCP_PWRCTRL = "High" , Vo = 1.05V (SNB)
VCCP_PWRCTRL = "Low" , Vo = 1V (IVB)

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+1.05V_RUN_VTT

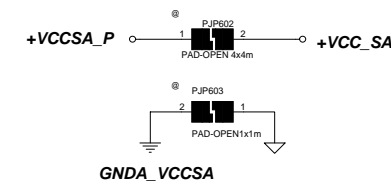
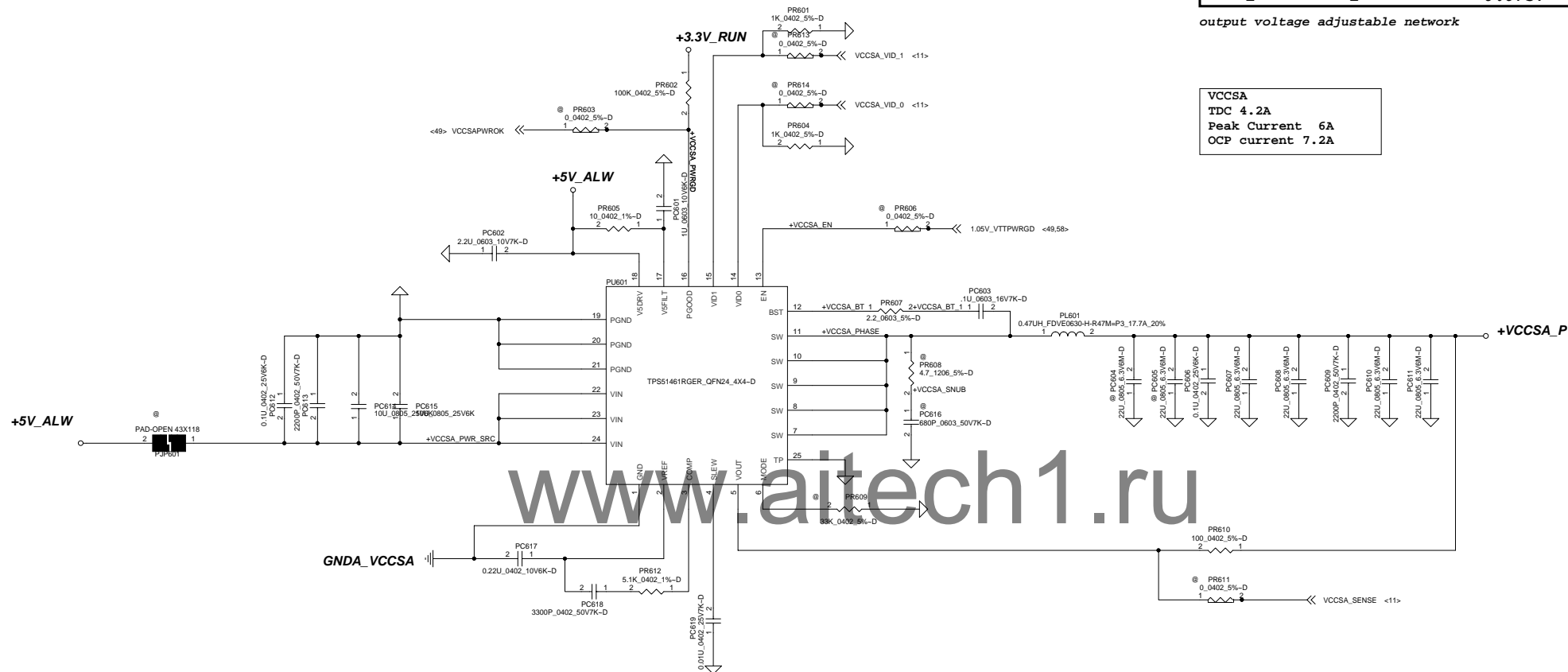
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VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

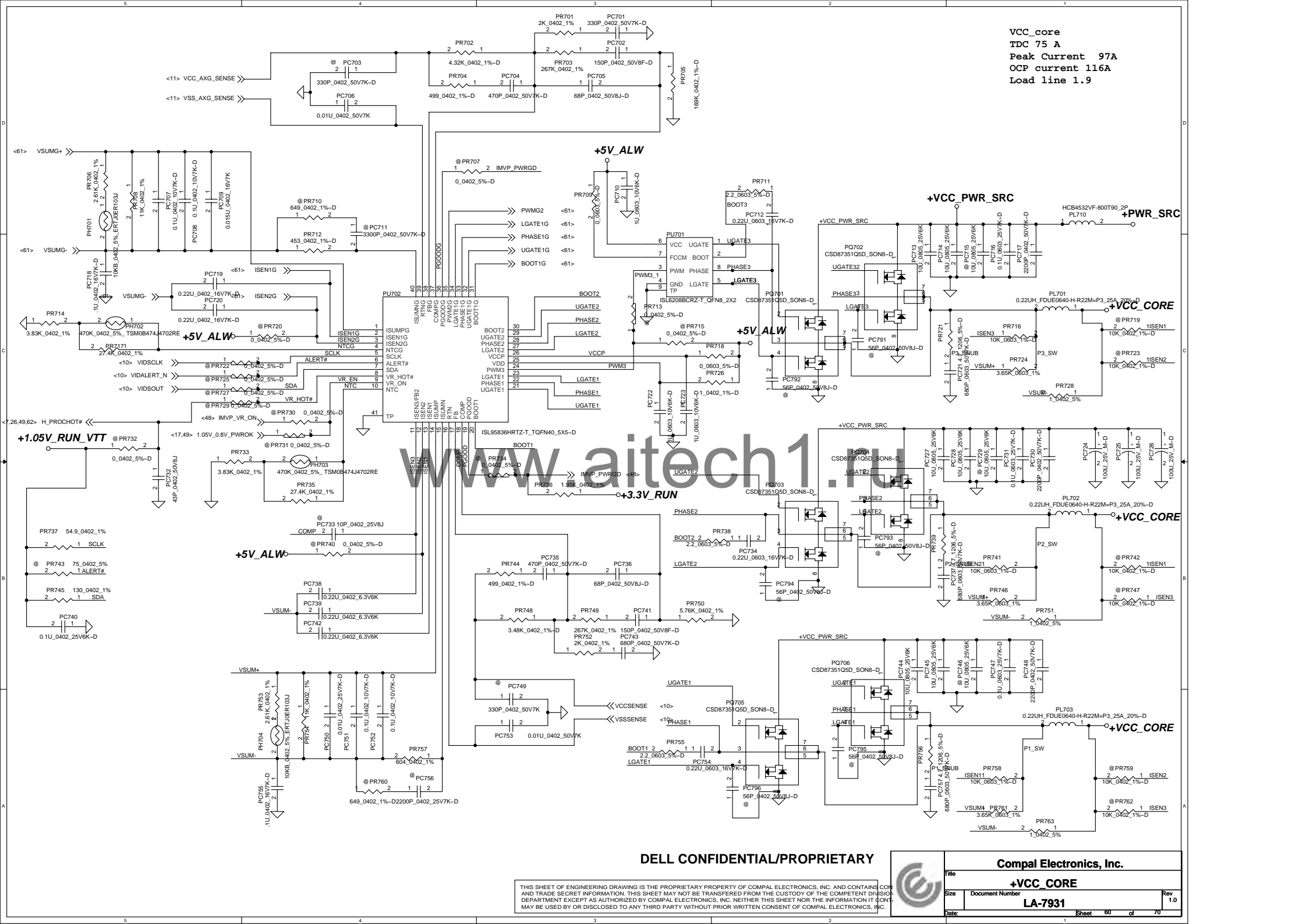
VCCSA
TDC 4.2A
Peak Current 6A
OCP current 7.2A



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File	+VCC_SA
Size	Document Number
	LA-7931
Date:	Monday, July 23, 2012
Sheet	59 of 70
Rev	1.0

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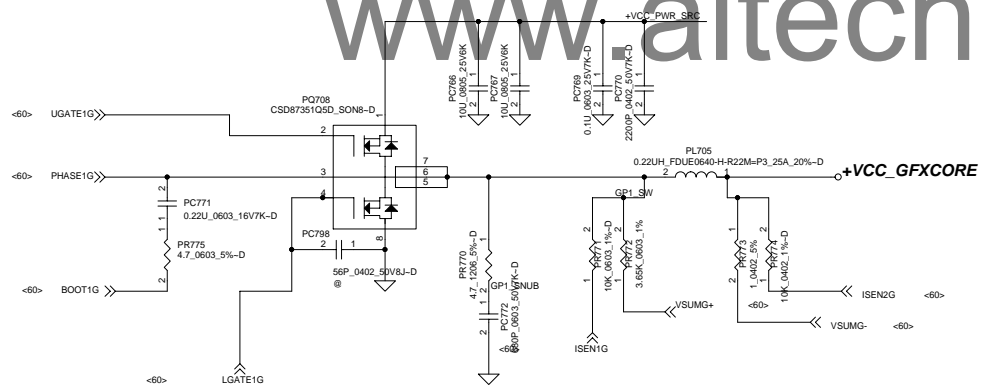
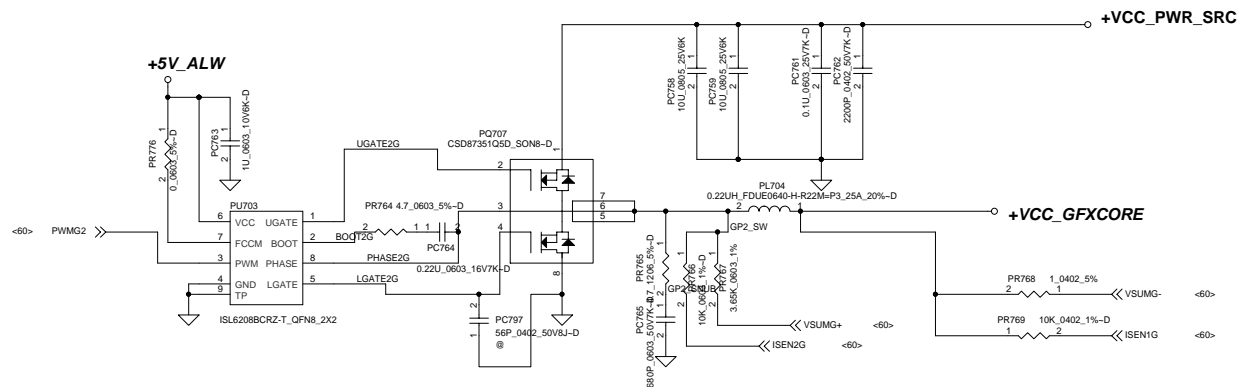


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+VCC_CORE	
File	LA-7931
Size	Document Number
Date	Rev 1.0
Sheet 60 of 70	


VCC_GFXCORE
TDC 38A
Peak Current 46A
OCP current 57.18A
Load line 3.9



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		File		+VCC_GFXCORE	
		Size	Document Number	LA-7931	
Date:		Sheet		61	of 70
				Rev	1.0

E2 AC_OK=17.7 Volt

PR913
TI bq24745 = 316K
Intersil ISL88731 = 226K
Maxim = 383K

Iada=0-9.23A(180W)

Vref
TI bq24747 = 3.3V
Intersil ISL88731C = 3.2V
VDDP
TI bq24747 = 6V
Intersil ISL88731C = 5.1V

Maximum charging current is 7.2A

DYN_TUR_CURRENT_SET#	
150W	High
180W	Low

Adapter Protection Circuit for Turbo Mode

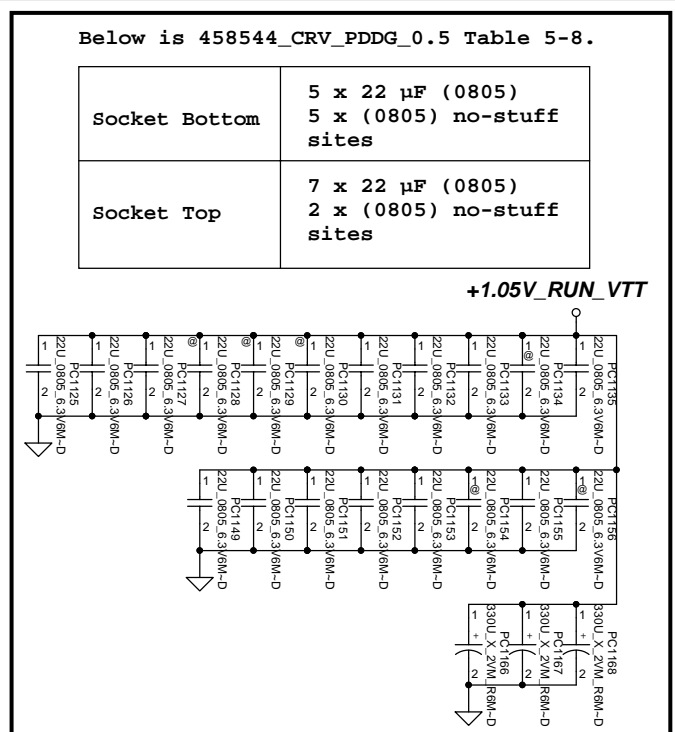
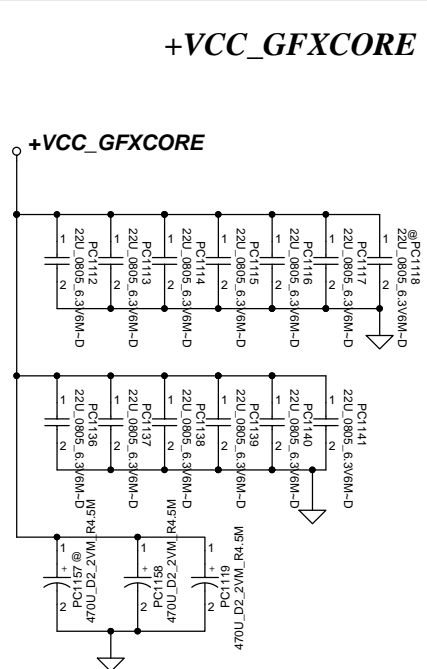
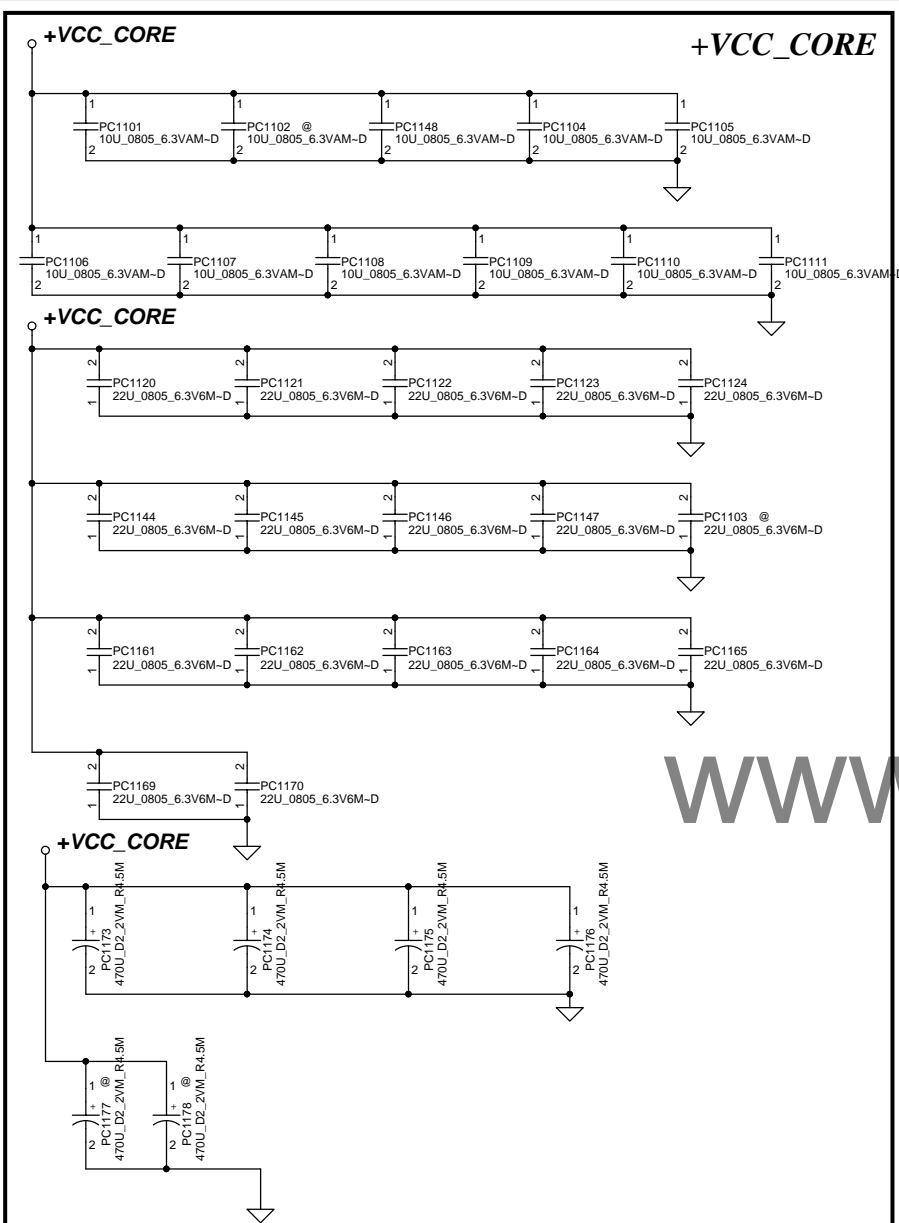
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Charger

File
Size
Document Number
LA-7931
Date: Monday, July 23, 2012
Sheet 62 of 70

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LA-7931

Monday, July 23, 2012


Sheet 64 of 70

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	62	PWR	10/11	Intersil	Remove Docking current sense voltage division	Remove PR946, PR948 and PR947	X01
2	53	PWR	10/14	Compal	Change RTC battery connector	Change to SP02000R000	X01
3	53	PWR	10/14	Compal	Add control singnal to control S5 power consumption	Add PR23 to connect PCH_ALW_ON singal	X01
4	62	PWR	10/14	Compal	Change H_PROCHOTH voltage source of Compare reference	PR937 connect to 2VREF_6182	X01
5	53	PWR	10/25	Compal	Change PQ5 Package for layout space	Change footprint from T0252 to S08_5P	X01
6	60	PWR	11/01	Compal	Change PC707 PC751 footprint from 0603 to 0402	Change PC707 PC751 footprint to 0402	X01
7	61	PWR	11/01	Compal	Remove PJP702	Remove PJP702	X01
8	54,55,57,58,60,61,62	PWR	11/07	Compal	Low side MOSFET Gate induce voltage	Reserve PC198,PC199,PC299,PC499,PC599,PC791,PC792,PC793,PC794,PC795,PC796,PC797,PC798,PC999	X01
9	53	PWR	11/07	Compal	Reserve 10u and 0.1u Cap with MXM_pwr_src	Reserve PC30 and PC31	X01
10	53	PWR	03/01	Compal	Reserve PD7 for ESD requirement	Reserve PD7	X03
11	53,54,55,56,57,58,59,59,60,61,62,63	PWR	04/03	Compal	Change 0 Ω footprint to R0402_0ohm	PR1002,PR1004,PR1006,PR1007,PR1008,PR1009,PR1010,PR1012,PR1014,PR1015,PR1016,PR1017,PR1019,PR1020,PR1021,PR1022,PR1023,PR1024,PR1025,PR1027,PR1029,PR105,PR118,PR206,PR214,PR226,PR23,PR307,PR311,PR404,PR504,PR509,PR510,PR6,PR603,PR606,PR611,PR613,PR614,PR713,PR722,PR725,PR727,PR729,PR731,PR734,PR902,PR903,PR910,PR915,PR935,PR938	X06
12	59	PWR	04/03	Compal	Change PL601 Footprint for DFB issue	Change PL601 footrpint to TAI-T_VMPI0703AR-1ROM-Z01_2P	X06
13	53	PWR	04/03	Compal	Battery ESD protect with ESD diode	PD3.3 connect with PBATT1.7	X06
14	54,62	PWR	04/03	Compal	Remove jump of co-lay with input choke	Remove PJP901 and PJP101	X06
15	60	PWR	05/04	Compal	Change PL710 Footprint for DFB issue	Change PL701 footrpint to KC_FBMA-L11-453215-121LMA90T_2	X07
16	60	PWR	05/14	Compal	Change 0 Ω footprint to R0402_0ohm	PR928	X07

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Compal Electronics, Inc.			
Title PWR_PIR 1			
Size	Document Number LA-7931		Rev 1.0
Date:	Monday, July 23, 2012		Sheet 65 of 70

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	16	HW	2011/09/01	COMPAL	correct MXM LVDS signals.	Swap CHA and CHB signals on JMXM1.	0.2(X00)
2	51	HW	2011/09/01	COMPAL	Add current limilt R for Breath LED.	Add R956(374ohm).	0.2(X00)
3	46	HW	2011/09/04	COMPAL	for layout routing easy.	Move D33,C702,CE6 from JDOCK1.146-148 to JDOCK1.149-151. JDOCK1.146-148 change to dummy pin.	0.2(X00)
4	51	HW	2011/09/06	Lite-on	to meet LED min workable current(2mA).	Change R934,R939,R942,R955,R941 from 2.2kohm to 1.2kohm. R943 from 2.2kohm to 374ohm.	0.2(X00)
5	27	HW	2011/09/06	COMPAL	Add MXM DDC signals pull up R.	pop R1121,R1122.	0.2(X00)
6	45	HW	2011/09/09	COMPAL	Add DOCK DP DDC signals control circuit.	Add R2144-R2157,C1331,C1332,Q333-Q336,R2161-R2164,Q337.	0.3(X01)
7	41	HW	2011/09/14	COMPAL	modify JUSH1 pin define for meeting USH/B JUSH1 pin define change.	change JUSH1 pin define.	0.3(X01)
8	50	HW	2011/09/19	COMPAL	modify JBT1 pin define for meeting BT connector change.	Swap JBT1 pin1-pin12 pin define to pin12-pin1.	0.3(X01)
9	46,28,50	ME	2011/09/27	COMPAL	Change connector follow connector list 0913A.	Change JDOCK1 to WD2F144WB5R400,JLVDS1 to 50398-04071-001,JBT1 to 50450-0127N-001.	0.3(X01)
10	52	HW	2011/09/27	COMPAL	+3.3V_RUN boot leakage.	Pop R929,Q69.	0.3(X01)
11	20,48,28	HW	2011/09/28	DELL	Drop touch panel.	Remove net "USBP13-,USBP13+,TOUCH_SCREEN_PD#" and L11,R429,R430,D86,R419, JTS1.	0.3(X01)
12	46	HW	2011/09/28	COMPAL	Add pull-down R for DPC_GPU_HPD.	Add R773(100K ohm).	0.3(X01)
13	34	HW	2011/09/29	COMPAL	Change the R518 value to meet the PS8336B input high-level voltage.	Change R518 from 100k to 10kohm.	0.3(X01)
14	52	HW	2011/09/29	COMPAL	Solve S4/S5 +MXM_PWR_SRC leakage in DC mode.	Change R940 pin1 connect from +PWR_SRC_S to +PWR_SRC_MXM.	0.3(X01)
15	49,17,18	HW	2011/10/04	COMPAL	Crystal EA.	Change C743,C741 from 22pF to 39pF, CH2,CH3 from 15pF to 18pF, CH18,CH19 from 12pF to 10pF.	0.3(X01)
16	17	HW	2011/10/12	COMPAL	Debug component control for pop them until ST.	Add JTAG@ for RH288,RH59,RH44,RH45,RH43,RH47-RH49.	0.3(X01)
17	48	HW	2011/10/12	COMPAL	Wireless switch needs to be pulled to ALW, Without it being pulled to ALW fail AONC will work incorrect.	Add R2158 let WIRELESS_ON# /OFF pull up to ALW, no stuff R766	0.3(X01)
18	51	HW	2011/10/12	COMPAL	Solve Breath LED flicker when AC-in plug and correct Breath LED top and side view work behavior.	Add Q327 and use "MASK_BASE_LEDS#" to control Breath LED top view. use "SYS_LED_MASK#" to control Breath LED side view.	0.3(X01)
19	28	HW	2011/10/12	COMPAL	JLVDS1 connector change,then GND shield shift(different from original).because JLVDS1 and JLVDS2 co-lay,we need change pin define.	JLVDS2 pin41,42 change to EDP_LVDS_A3-,EDP_LVDS_A3+, pin43-pin46 change to GND.	0.3(X01)
20	34	HW	2011/10/12	COMPAL	Choice DDC active buffer mode.and control switching Mode.	Pop R68 and non-pop R58.	0.3(X01)
21	50	HW	2011/10/13	COMPAL	To meet intel spec: T235(power off)= min 40ns). T08a(power on)= max 90ms.	change U4 from RT9801AGE to RT9818A-44GU3,R1622 to 100kohm.add R2159. remove R2129-R2134. pop R2142 and non-pop R1623.	0.3(X01)
22	14	ME	2011/10/13	COMPAL	Change connector follow connector list 1005A.	Change JDIMM3 to 2-2013310-1.	0.3(X01)
23	38	HW	2011/10/19	COMPAL	LAN EA.	Change T156 to SP050006P0L.	0.3(X01)
24	22	HW	2011/10/19	COMPAL	for solving dispaly ripples. 1/2	Change LH1 to 4.7uH inductor.	0.3(X01)
25	40	HW	2011/10/25	COMPAL	NEC_TOKIN shortage issue for the flood in Tailand.	Change C323,C324 to SGA0000370L(Panasonic).	0.3(X01)
26	34	HW	2011/10/25	COMPAL	HDMI EA.	pop R451-R456,R458,R459 and non-pop L19,L23,L24,L25.	0.3(X01)
27	51	HW	2011/10/25	COMPAL	improve BT_LED behaviour abnormal(BT_LED must dark) in S3/S4/S5.	change R938 PU from +3.3V_RUN to +3.3V_ALW.	0.3(X01)
28	38,51	HW	2011/10/26	COMPAL	for ESD Hi-Pot fail.	change JLOM1 "pin14 and pin15" from "GND_CHASSIS1 and GND_CHASSIS" to GND. change H5 to NPTH.	0.3(X01)
29	41	HW	2011/10/26	COMPAL	TPM chip to new version chip due to OS Win8 supported problem	Change U39 TPM solution to new p/n: SA00004WQ10	0.3(X01)
30	51	ME	2011/10/26	COMPAL	screw hole change follow 1021A ME drawing.	Change H5 to 3P2X6P2 and H18,H19,H23,H24 to 4P1.	0.3(X01)
31	51	HW	2011/10/28	COMPAL	Solve Breath LED flicker when AC-in plug,follow E4 solution.	Remove Q327 and modify EC code from PWM Output to GPIO input on ECE5048 (GPIO3/PWM4).	0.3(X01)
32	52	HW	2011/10/28	COMPAL	For Inrush current issue.	Change C1274 from 470pF to 2200pF for meeting OCP.	0.3(X01)

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Compal Electronics, Inc.		
Title EE_PIR 1		
Size	Document Number LA-7931P	Rev 1.0
Date	Monday, July 23, 2012	
Sheet		66 of 70

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
33	52	HW	2011/10/28	COMPAL	For smart card detect issue.	Change C767 from 4700pF to 470pF for turning proper +3.3V_SUS timing begin to +3.3V_RUN.	0.3(X01)
34	14	HW	2011/10/28	COMPAL	For DFX issue.	Change CD45 from 0603 size to 0402 for easy move to keep away battery connector.	0.3(X01)
35	47, 46, 32 40, 29	HW	2011/10/28	COMPAL	For ESD request.	Change D97, D33, D91, D92 to non-pop. D14, D16 change main source(SC30000250L) to SC300002F0L and D88, D89 change main source(SCA00000T0L) to SC300002F0L.	0.3(X01)
36	46	HW	2011/10/31	COMPAL	EMI request, add 33ohm for DOCK DVI signals.	Add R2160, R2165~R2179(33ohm) for DOCK DVI port A,B.	0.3(X01)
37	34	HW	2011/10/31	COMPAL	EMI request, add reserve C(3.3pF) for HDMI signals.	Add reserve C1333~C1340(3.3pF) for HDMI signals.	0.3(X01)
38	21	HW	2011/11/2	COMPAL	PCH has internal pull up 20k ohm on (GPIO27)	No stuff RH175	0.3(X01)
39	21	HW	2011/11/2	COMPAL	Power saving	RH362 change from 10K to 100K	0.3(X01)
40	22	HW	2011/11/2	COMPAL	for solving dispaly ripples. 2/2	Change CH36 to 22uF_0805 size.	0.3(X01)
41	49	HW	2011/11/2	COMPAL	Change board ID to X01	Change R875 to 130K	0.3(X01)
42	52	HW	2011/11/2	COMPAL	Power saving	R935 change from 20K to 100K	0.3(X01)
43	33, 46	HW	2011/11/2	COMPAL	reduce layout via.	MXM DP lane for Docking direct connect to JDOCK1.	0.3(X01)
44	45	HW	2011/11/3	COMPAL	remove double pull low R.	remove R2144, R2154.	0.3(X01)
45	16	HW	2011/11/3	COMPAL	only 10-bits panel use.	change R2095, R2096 to 6@ group.	0.3(X01)
46	49	HW	2011/11/3	COMPAL	SMBUS EA.	change R838, R841 to 2Kohm for rise timing fail.	0.3(X01)
47	32	LAYOUT	2011/11/7	COMPAL	Add TEST point for JCRT PIN11.	Add CRT_11 net and test point(T61) for JCRT1.11.	0.3(X01)
48	33	HW	2011/11/7	COMPAL	Add space for easy to layout.	Remove R2081~R2088 and remove Net DPC_DOCK_LANE_P0~P3, DPC_DOCK_LANE_N0~N3.	0.3(X01)
49	40	HW	2011/11/7	Parade	USB3.0 EA fine tune(TX:EQ-->9.5dB, DE-->3.5dB; RX:EQ-->7.5dB, DE-->5dB).	pop R22, R18, R30, R28 and change R2141 from 4.99kohm to 4.7kohm.	0.3(X01)
50	30	HW	2011/11/8	H.ELE	Vender suggested changed small size from 5.0*3.2mm to 3.2*2.5mm.	Change Y7 from SJ100006R00 to SJ10000CZ0L, C1225 from 10pF to 15pF, C1226 from 10pF to 12pF.	0.3(X01)
51	30	HW	2011/11/9	compal	for satisfy ME space limilt.	Change C324 size from D2 to B2.	0.3(X01)
52	46	HW	2011/11/10	COMPAL	Just reserve R for EMI team to test DOCK DVI signals.	Change R2160, R2165~R2179 to 0ohm for DOCK DVI port A,B.	0.3(X01)
53	40	HW	2011/12/30	COMPAL	source request	change USB PWR SW from TPS2560 (U45) to G54712P81H (U642 U643)	0.4(X01)
54	46	EMI	2011/12/30	COMPAL	EMI issue.	Swap USB signal from port 8 to port 4 on JDOCK1.66 & JDOCK1.68	0.4(X01)
55	42	EMI	2011/12/30	COMPAL	EMI issue.	Swap USB signal from port 4 to port 8 on JMINI1.36 & JMINI1.38	0.4(X01)
56	35	HW	2011/12/30	COMPAL	2nd source.	add R2180 ~ R2184, R2189 ~ R2193 for SATA redriver(U26, U637) 2nd source and change R1206 from 4.99K ohm to 5.1K ohm.	0.4(X01)
57	41	HW	2012/01/02	COMPAL	Solve +3.3V_RUN Giltch in S5 when AC plugging in.	add R2185, R2186, D103 to SP_TPM_LPC_EN.	0.4(X01)
58	30	HW	2012/01/02	COMPAL	Prevent AUX swing overshoot.	add R2187, R2188 on AUX signal.	0.4(X01)
59	52	HW	2012/01/02	COMPAL	Power sequencing meet 0.7V between +PCH_V5REF_RUN and +3.3V_RUN.	change C1274 from 2200P to 3300P, and No stuff R2127	0.4(X01)
60	34	HW	2012/01/02	COMPAL	HDMI no voice issue	stuff R58.	0.4(X01)
61	51	HW	2012/01/03	COMPAL	Setup Volume mute LED control same as Volume up & down	No stuff Q84B	0.4(X01)
62	46	HW	2012/01/03	COMPAL	EMI request add 33ohm for DOCK DVI signals.	change R2160, R2165 ~ R2179 from 0 ohm to 33 ohm.	0.4(X01)
63	34	HW	2012/01/03	COMPAL	EMI request for HDMI.	stuff L19, L23, L24, L25, No stuff R451~R456, R458, R459	0.4(X01)
64	32	HW	2012/01/03	COMPAL	EMI request for CRT.	change CAP from 3.3P to 12P (C12, C13, C21), and stuff.	0.4(X01)
65	28	HW	2012/01/03	COMPAL	EMI request for Webcam.	stuff L10, No stuff R427, R428	0.4(X01)
66	30, 31	HW	2012/01/04	COMPAL	RGB panel sequencing issue.	change power rail from +3.3V_RUN to +3.3V_AVDD on R2039.1, R2040.1, R2038.1, C1227.1, U631.3 Remove C1269, C1270 add L57	0.4(X01)

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Compal Electronics, Inc.

Title		
EE_PIR 2		
Size	Document Number	Rev
	LA-7931P	1.0
Date:	Monday, July 23, 2012	Sheet 67 of 70

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
67	16	HW	2012/01/04	COMPAL	Height limitation issue.	change cap from SE142106M8L(1206) to SE000000QK0L(0805)	0.4(X01)
68	40	HW	2012/01/05	COMPAL	change main source.	change main source from SLG55584A to MAX14618 on U2.	0.4(X01)
69	33	HW	2012/01/05	COMPAL	Remove DMC function.	Remove U14, R329-R335, R337, R338, R342-R345, R2091, R2092, C396, C399-C401, C267, C269, C273-C278.	0.4(X01)
70	42	HW	2012/01/05	COMPAL	Remove DMC function.	Remove JMINI1, R493.	0.4(X01)
71	51	ME	2012/01/09	COMPAL	update ME drawing.	Remove H3.	0.4(X01)
72	40	ME	2012/01/09	COMPAL	update ME drawing.	change JUSB1, JUSB2 from FOX_UEA111Y1-C5BDA-7H to FOX_UEA111Y1-C1BD1-7H	0.4(X01)
73	17	ME	2012/01/09	COMPAL	update ME drawing.	change JSPI1 from HRS_FH12-16S-0P5SH(55)-D to TYCO_1-2041070-6-D.	0.4(X01)
74	25	ME	2012/01/09	COMPAL	update ME drawing.	change JFAN1, JFAN2 from ACES_50228-0047N-001 to ACES_50450-0067N-001.	0.4(X01)
75	30	HW	2012/01/10	COMPAL	prevent current leakage.	Change Pull up +3.3V_RUN to +3.3V_AVDD on R2036 and R2037.	0.4(X01)
76	49	HW	2012/01/10	COMPAL	change Board ID to X02.	change R875 to 62K ohm.	0.4(X01)
77	33	HW	2012/01/10	COMPAL	prevent material shortage for Thai flood.	change material from TC7SET04FU to NC7ST04P5X on U636.	0.4(X01)
78	28	HW	2012/01/10	COMPAL	prevent material shortage for Thai flood.	change material from TC7SET04FU to M74VHC1GT125DF2G on U3.	0.4(X01)
79	19,20,25, 37,49,50, 51	HW	2012/01/10	COMPAL	prevent material shortage for Thai flood.	change material from TC7SH08FU to 74AHC1G08GW on U7, U10, U15, U50, U58, UC4, UH3.	0.4(X01)
80	35,43	HW	2012/01/10	COMPAL	add X76 option for main source and 2nd source of SATA redriver .	add X761@ on R1201, R1202, R1206, R2136, R2139, R2140. add X762@ on R2180 ~ R2184, R2189 ~ R2193.	0.4(X01)
81	25	HW	2012/01/11	COMPAL	layout routing swap	change FAN conn from 4 pin to 6 pin, and swap pin 1, pin6 for JFAN1, JFAN2.	0.4(X01)
82	16	HW	2012/01/11	COMPAL	For NVIDIA request	add R2194, R2195 (No stuff) and pull up to +3.3V_MXM on JMXM1B.268, JMXM1B.270	0.4(X01)
83	32	HW	2012/01/18	COMPAL	EMI request.	change CAP to 22P (C20,C22,C23) and 10P (C12, C13, C21), and all stuff.	0.4(X01)
84	46	HW	2012/01/20	COMPAL	Solve dock detection issue.	change R755 from 100K to 10K.	0.4(X01)
85	49	HW	2012/01/20	COMPAL	Avoid material mixture with E3 project 5055 devices.	change MEC5055 from SA00003TZ1L to SA00003TZ2L.	0.4(X01)
86	11,28,36 44,52	HW	2012/01/20	COMPAL	Change RC value at Gate of MOS Load SW to modify power rail soft start timing.	RC73 from 100K to 330K; RC79 from 330K to 1M; CC71 from 0.1u to 0.022u R412 from 100K to 470K; R1632 from 1M to 4.7M; C293 from 0.1u to 0.022u R515 from 100K to 470K; R2126 from 1M to 4.7M; C416 from 0.1u to 0.022u R731 from 100K to 470K; R1628 from 1M to 4.7M; C651 from 4700p to 220p R737 from 100K to 470K; R1629 from 1M to 4.7M; C652 from 4700p to 220p R917 from 100K to 470K; R1617 from 1M to 4.7M; C770 from 4700p to 220p R930 from 100K to 470K; R1611 from 470K to 2.2M; C773 from 2200p to 100p R2067 from 100K to 470K; C1272 from 2200p to 220p R2069 from 100K to 470K; C1274 from 470p to 220p	0.4(X01)
87	16	HW	2012/02/29	COMPAL	For NVIDIA request	No stuff RV29	0.5(X01)
88	40	HW	2012/02/29	COMPAL	2nd source.	add R2196 ~ R2197, change power rail from +3.3V_RUN to +USB3 on U638.9 and U638.25	0.5(X01)
89	40	HW	2012/02/29	COMPAL	Reserve for samsung mobile issue.	add Q338 and No stuff.	0.5(X01)
90	51	HW	2012/03/01	COMPAL	change MOS to single package.	change Q84, Q339 from DMN66D0LDW to SSM3K7002FU.	0.5(X01)
91	25	HW	2012/02/29	COMPAL	change FAN conn.	change FAN conn from ACES_50450-0067N-001 to ACES_50271-0040N-001 on JFAN1, JFAN2	0.5(X01)

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Compal Electronics, Inc.			
Title EE_PIR 3			
Size	Document Number LA-7931P		Rev 1.0
Date: Monday, July 23, 2012		Sheet 68	of 70

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
92	40	HW	2012/03/01	COMPAL	change main source.	change main source from MAX14618 to SLG55584A on U2.	0.5(X01)
93	35	HW	2012/03/01	COMPAL	For SATA Gen2, Gen3 EA setting.	stuff R1173, R1204 and No stuff R1206.	0.5(X01)
94	43	HW	2012/03/01	COMPAL	For SATA Gen2, Gen3 EA setting.	stuff R2135, R2138 and No stuff R2139.	0.5(X01)
95	31	HW	2012/03/01	COMPAL	Meet RGB panel sequencing.	stuff L56 and No stuff L57.	0.5(X01)
96	28	HW	2012/03/01	COMPAL	change to new manufacturing technology.	change from RB751V-40GTE to RB751VM-40TE on D53,D64,D66,D67,D69,D100, D101.	0.5(X01)
97	29	HW	2012/03/02	COMPAL	According to new EIA rule.	Change U627 from PS8330BQFN48GTR-A0 to PS8330BQFN48GTR2-A0.	0.5(X01)
98	28	HW	2012/03/05	COMPAL	Solve LVDS cable burn out issue	change JLVDS1_4 and JLVDS2_4 to NC	0.5(X01)
99	16	HW	2012/03/05	COMPAL	Meet high level on DGPU_PEX_RST# for N14P.	change RV29 to 750 ohm and stuff.	0.5(X01)
100	40	ME	2012/03/05	COMPAL	Update Conn list.	change JUSB1, JUSB2 from UEA111Y1-C1BD1-7H to AUSB0041-P001A.	0.5(X01)
101	34	HW	2012/03/05	COMPAL	Meet AMD HDMI 297 MHz EA setting.	stuff R71, R65, R67.	0.5(X01)
102	40	HW	2012/03/06	COMPAL	2nd source.	change power rail from +3.3V_RUN to +USB3 on R26.1	0.5(X01)
103	51	ME	2012/03/07	COMPAL	ME request.	add H27.	0.5(X01)
104	12	HW	2012/03/08	COMPAL	layout space limitation.	Remove RD12, RD13.	0.5(X01)
105	13	HW	2012/03/08	COMPAL	layout space limitation.	Remove RD21, RD22.	0.5(X01)
106	28	HW	2012/03/08	COMPAL	Solve LVDS cable burn out issue.	add one test point on JLVDS1.4 and JLVDS2.4	0.5(X01)
107	28	HW	2012/03/13	COMPAL	Wrong CPN for prefix number.	change CPN from SM01000700L to SM070001I0L on L10.	0.5(X01)
108	11	HW	2012/03/13	COMPAL	Solve backdrive (follow B4).	change CPN from SB000000B00 to SB000000RV00 on QC3.	0.5(X01)
109	16	HW	2012/04/02	COMPAL	Solve AUX signal pull to different power rail.	Change power rail from +3.3V_RUN to +3.3V_AVDD.	0.6(X02)
110	28	EMI	2012/04/02	COMPAL	EMI request.(RGB noise coupling to LVDS cable 224MHz)	Reserve C1341, C1342 on LCD_SMBCLK and LCD_SMBDAT.	0.6(X02)
111	7~52	HW	2012/04/05	COMPAL	short all reserved 0 Ohm resister.	RC24,RC27,RC17,RC18,RC25,RC68,RC69,RC83,RD1,RD2,RD7,RD14, R1157,R1158, RD15,RD16,RD23,RD24,RD25, RD32, RD33, RD34, RD39, RD40, R1169, R1624, R1626 R1970, RH286, RH290, RH307, RH308, RH82, RH83, RH85, RH86, RH88, RH90, RH92, R2089, RH93, RH95, RH96, RH280, RH281, RH359, RH113, RH323, RH116, RH117, R2090, R2105, R2142 RH320, RH120, RH121, RH122, RH334, RH343, RH335, RH336, RH338, RH339, RH341, RH356, RH259, RH150, RH201, R1187, R551, R552, R2159, RC29, RC34, RC40, R555, R1144, R702, R707, R709, R703, R724, R730, R713, R797, R771, R741, R815, RC9, RH1, R1068, R867, R853, R855, R862, R1180, R1633, R781, R808, RH2, RH309, RH337, R2072, R289, RH202, RH205, RH211.	0.6(X02)
112	26	HW	2012/04/05	COMPAL	Remove current sensor function.	No stuff R1974, R1975, C16, C17, C361, C363.	0.6(X02)
113	25	HW	2012/04/09	COMPAL	change VSET from 88 to 93	change R406 from 953 ohm to 1.33K ohm.	0.6(X02)
114	49	HW	2012/04/09	COMPAL	change Board ID to X03.	change R875 from 62K ohm to 33K ohm.	0.6(X02)
115	29	HW	2012/04/09	COMPAL	[DF543750]DP->HDMI/DP->S-DVI dongle no function on NV units.	Add TMDS DDC PU schematic on DP port that include Q339, Q340, R2198~2201, C1343.	0.6(X02)
116	42	HW	2012/04/09	COMPAL	Add WiGig card function.	Add net name WiGi_RADIO_DIS#_R on JMINI4.32, net name BT_RADIO_DIS#_R on JMINI4.51, and reserve R2204, R2205, D104, D105.	0.6(X02)
117	48	HW	2012/04/09	COMPAL	Add WiGig card function.	change net name from VOL_MUTE_LED# to WiGi_RADIO_DIS# on U46.A1 PU 100K ohm on net WiGi_RADIO_DIS# and BT_RADIO_DIS#.	0.6(X02)

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Compal Electronics, Inc.		
Title EE_PIR 4		
Size	Document Number LA-7931P	Rev 1.0
Date	Monday, July 23, 2012	
Sheet		69 of 70

DELL CONFIDENTIAL/PROPRIETARY

Title			
EE_PIR 4			
Size	Document Number	Rev	
	LA-7931P	1.0	
Date:	Monday, July 23, 2012	Sheet	70 of 70

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